HOLT INTEGRATED CIRCUITS INC.

HI-1585

March 2017

MIL-STD-1553 / 1760
3.3V Dual Transceiver with Tail-Off Control

DESCRIPTION

The HI-1585 is an ultra-low power CMOS dual transceiver designed to meet the requirements of the MIL-STD-1553 and MIL-STD-1760 specifications.

The transmitter section of each bus takes complementary CMOS / TTL Manchester II bi-phase data and converts it to differential voltages suitable for driving the bus isolation transformer. Separate transmitter inhibit control signals are provided for each transmitter.

The receiver section of the each bus converts the 1553 bus bi-phase analog signals to complementary CMOS / TTL data suitable for input to a Manchester decoder. Each bus has its own Receive Enable input, which forces both receive output signals to the bus idle state (logic "0") when disabled.

To reduce end-of-transmission residual voltage offset (”tail-off”), logic-level transmit signal inputs can be clocked-in to synchronize their rise/fall transitions. This compensates for timing mismatch or transmit signal path propagation differences caused by board layout.

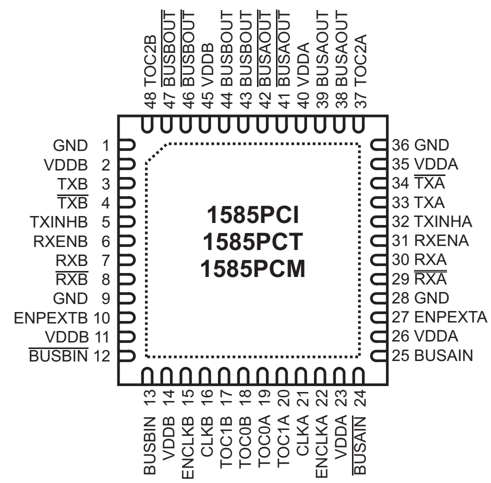
When sub-optimal board design consistently presents tail-off magnitudes close to or exceeding mandatory limits, another unique option lets the user select a bus-specific level of digital tail-off compensation.

The HI-1585 also provides optional Receive output pulse extension. With traditional MIL-STD-1553 transceivers, low amplitude receive signals can result in RX/nRX pulses less than 100ns wide. When this feature is enabled, RX/nRX output pulse widths do not drop below 300ns, greatly simplifying decoder design and enhancing noise performance.

APPLICATIONS

- MIL-STD-1553 Terminals
- Flight Control and Monitoring
- Radar Systems
- ECCM Interfaces
- Stores Management
- Test Equipment
- Sensor Interfaces
- Instrumentation

PIN CONFIGURATION



48 Pin Plastic 6mm x 6mm Chip-Scale Package (QFN)

FEATURES

- Compliant to MIL-STD-1553A and B, MIL-STD-1760 and ARINC 708A
- 3.3V single supply operation
- Smallest transceiver footprint available in 6mm x 6mm 48-pin plastic chip-scale package (QFN)
- Input data synchronization.
- Tail-off compensation control.
- Receiver output pulse-width extension control.

PIN DESCRIPTIONS

PIN	SYMBOL	FUNCTION	DESCRIPTION
1	GND	power supply	Ground
2	VDDB	power supply	+3.3 volt power for transceiver B
3	TXB	digital input	Transmitter B digital data input, non-inverted Internal pull-down resistor
4	$\overline{TXB}$	digital input	Transmitter B digital data input, inverted Internal pull-down resistor
5	TXINHB	digital input	Transmit inhibit, bus B. If high BUSBOUT, $\overline{BUSBOUT}$ disabled Internal pull-down resistor
6	RXENB	digital input	Receiver B enable. If low, forces RXB and $\overline{RXB}$ low Internal pull-up resistor
7	RXB	digital output	Receiver B output, non-inverted
8	$\overline{RXB}$	digital output	Receiver B output, inverted
9	GND	power supply	Ground
10	ENPEXTB	digital Input	Enable pulse extension for receiver B Internal pull-up resistor
11	VDDB	power supply	+3.3 volt power for transceiver B
12	$\overline{BUSBIN}$	analog input	MIL-STD-1553 bus input B, negative signal
13	BUSBIN	analog input	MIL-STD-1553 bus input B, positive signal
14	VDDB	power supply	+3.3 volt power for transceiver B
15	ENCLKB	digital input	Enable input synchronization for transmitter B Internal pull-down resistor
16	CLKB	digital input	Synchronization clock input for transmitter B Internal pull-down resistor
17	TOC1B	digital input	Tail-off adjust transmitter B. (See Table 2) Internal pull-down resistor
18	TOC0B	digital input	Tail-off adjust transmitter B. (See Table 2) Internal pull-down resistor
19	TOC0A	digital input	Tail-off adjust transmitter A. (See Table 2) Internal pull-down resistor
20	TOC1A	digital input	Tail-off adjust transmitter A. (See Table 2) Internal pull-down resistor
21	CLKA	digital input	Synchronization clock input for transmitter A Internal pull-down resistor
22	ENCLKA	digital input	Enable input synchronization for transmitter A Internal pull-down resistor
23	VDDA	power supply	+3.3 volt power for transceiver A
24	$\overline{BUSAIN}$	analog input	MIL-STD-1553 bus input A, negative signal
25	BUSAIN	analog input	MIL-STD-1553 bus input A, positive signal
26	VDDA	power supply	+3.3 volt power for transceiver A
27	ENPEXTA	digital Input	Enable pulse extension for receiver A Internal pull-up resistor
28	GND	power supply	Ground
29	$\overline{RXA}$	digital output	Receiver A output, inverted
30	RXA	digital output	Receiver A output, non-inverted
31	RXENA	digital input	Receiver A enable. If low, forces RXA and $\overline{RXA}$ low Internal pull-up resistor
32	TXINHA	digital input	Transmit inhibit, bus A. If high BUSAOUT, $\overline{BUSAOUT}$ disabled Internal pull-down resistor
33	TXA	digital input	Transmitter A digital data input, non-inverted Internal pull-down resistor
34	$\overline{TXA}$	digital input	Transmitter A digital data input, inverted Internal pull-down resistor
35	VDDA	power supply	+3.3 volt power for transceiver A
36	GND	power supply	Ground
37	TOC2A	digital input	Tail-off adjust transmitter A. (See Table 2) Internal pull-down resistor
38	BUSAOUT	analog output	MIL-STD-1553 bus driver A, positive signal
39	BUSAOUT	analog output	MIL-STD-1553 bus driver A, positive signal
40	VDDA	power supply	+3.3 volt power for transceiver A
41	$\overline{BUSAOUT}$	analog output	MIL-STD-1553 bus driver A, negative signal
42	$\overline{BUSAOUT}$	analog output	MIL-STD-1553 bus driver A, negative signal
43	BUSBOUT	analog output	MIL-STD-1553 bus driver B, positive signal
44	BUSBOUT	analog output	MIL-STD-1553 bus driver B, positive signal
45	VDDB	power supply	+3.3 volt power for transceiver B
46	$\overline{BUSBOUT}$	analog output	MIL-STD-1553 bus driver B, negative signal
47	$\overline{BUSBOUT}$	analog output	MIL-STD-1553 bus driver B, negative signal
48	TOC2B	digital input	Tail-off adjust transmitter B. (See Table 2) Internal pull-down resistor

Table 1. Pin Descriptions

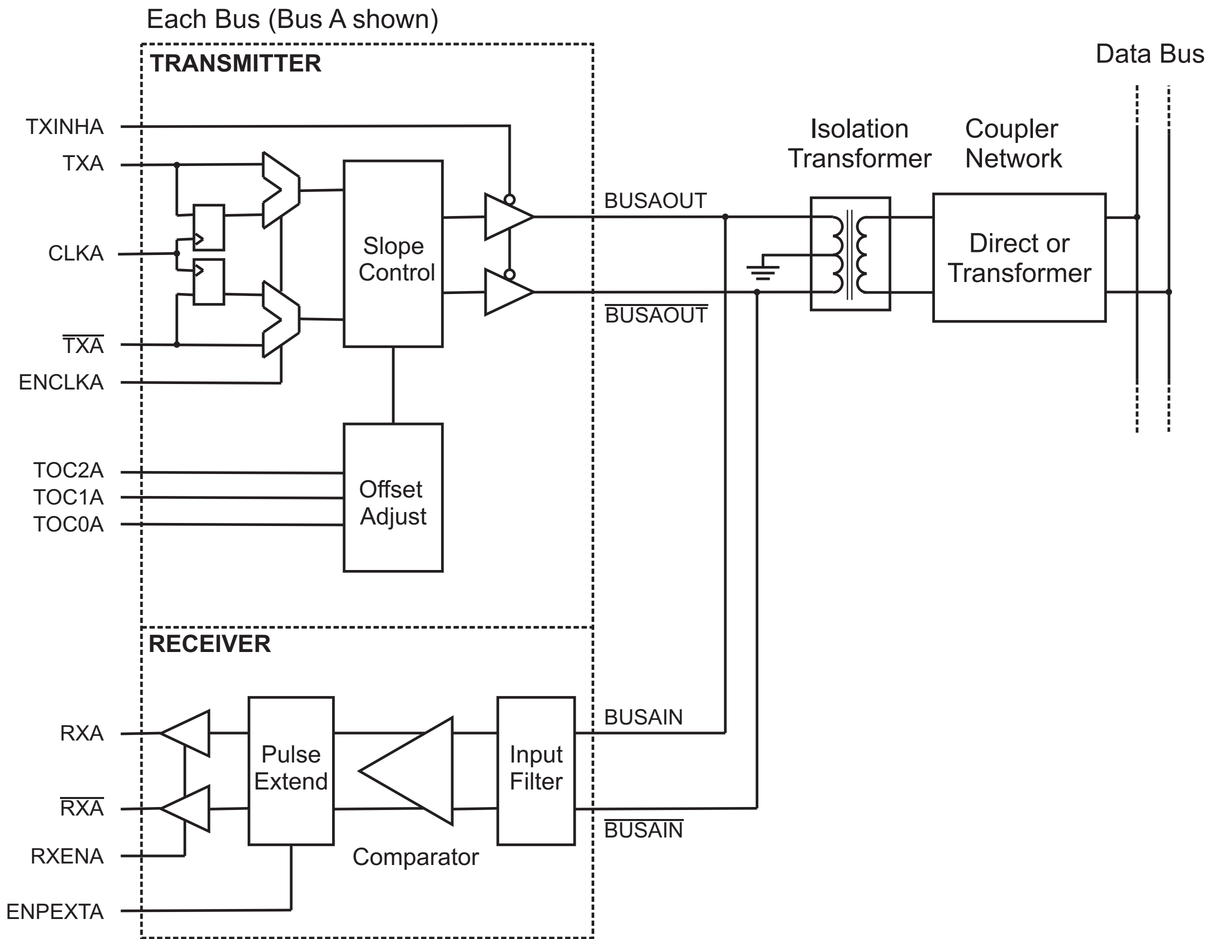


Figure 1. Block Diagram

FUNCTIONAL DESCRIPTION

The HI-1585 dual MIL-STD-1553 bus transceiver contains a differential voltage source driver and a differential analog bus receiver for each bus. It is designed for applications using a MIL-STD-1553B communications bus. The device generates a trapezoidal output waveform during transmission.

TRANSMITTER

For each bus, data input to the HI-1585 transmitter is a pair of complementary CMOS inputs TXA and $\overline{TXA}$ for Bus A, with a corresponding signal pair for Bus B. The transmitter accepts Manchester II bi-phase data and converts it to differential analog voltages on BUSAOUT and $\overline{BUSAOUT}$, or BUSBOUT and $\overline{BUSBOUT}$. The transceiver outputs are either direct- or transformer-coupled to the MIL-STD-1553 data bus. Both coupling methods produce a nominal voltage on the bus of 7.5 Volts peak to peak.

The transmitter is automatically inhibited and placed in the high impedance state when TXA and $\overline{TXA}$ (or TXB and $\overline{TXB}$) are both driven to the same logic state. A bus transmitter is also forced to the high impedance state when logic “1” is applied at the TXINHA (or TXINHB) transmit inhibit input, regardless of the TXA and $\overline{TXA}$ (or TXB and $\overline{TXB}$) input condition.

TRANSMIT-INDUCED TAIL-OFF (OFFSET)

A prevalent concern when designing MIL-STD-1553 terminals goes by a number of names, including transmit "output symmetry", "tail-off" and "offset". This is a transmit-induced phenomenon that occurs on the bus following long transmissions, when one or more design or operating factors are less than ideal. Slight imbalances in the transmitted analog signal voltage cause accumulation of energy in the terminal's isolation transformer. When transmission ends and the transceiver bus interface goes to the Standby or receive mode, a temporary DC voltage is expressed on the bus. This "tail-off" voltage can have positive or negative polarity; it decays exponentially, often persisting for 10 to 20µs depending on magnitude. See Figure 2. Good positive/negative signal matching (or short message transmissions) result in low tail-off magnitude, while serious mismatch problems combined with long transmissions can cause the DC stub voltage to approach or exceed 0.25 V peak-peak.

Design and product use factors that influence tail-off include:

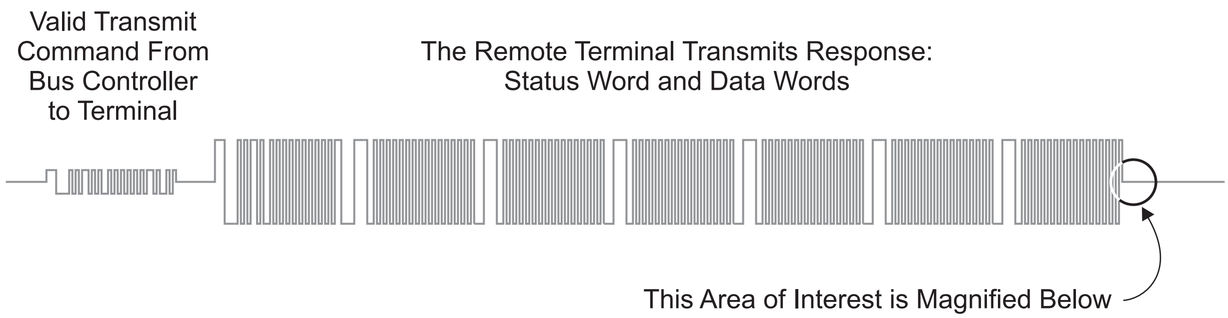
- the data patterns being transmitted. Some repeating data word values cause greater tail-off magnitude than random data or other repeating data patterns. For Holt transceivers, 32-word transmissions using repeating 0x0000 data usually give worst case tail-off magnitude
- timing skew for TX and $\overline{TX}$ input signals generated by the encoder
- mismatched conductor length or impedance between encoder and transceiver drive signal inputs for TX and $\overline{TX}$
- mismatched positive/negative drive voltage in the transceiver
- mismatched positive/negative rise and fall times in the transceiver
- poor signal path impedance matching between transceiver positive/negative drive output pins and the isolation transformer
- imbalance between positive/negative half-windings in the center-tapped isolation transformer.

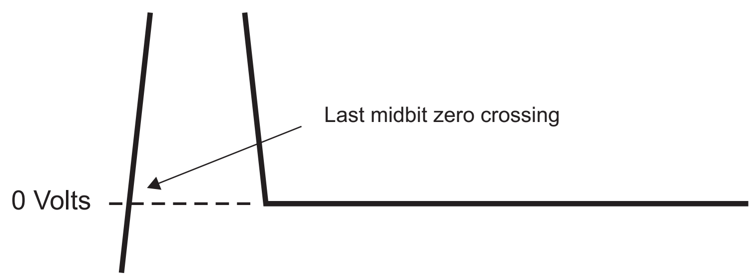
Holt carefully designs its MIL-STD-1553 transceivers for symmetry and matched positive/negative drive characteristics to minimize transceiver contribution to tail-off. We strongly urge designers to prioritize system topology and layout so that MIL-STD-1553 bus interface characteristics are considered first. All too often, it seems like 1553 bus interface is a late consideration, resulting in marginal performance (or worse) and considerable time wasted on redesign.

Ideally, the isolation transformer is located close to the 1553 bus cable termination connector. The transceiver should be close to the transformer with matched signal path conductors. The Manchester II encoder (often implemented in FPGA or CPLD) should be close to the transceiver and uses Hardware Description Language (HDL) that carefully matches positive/negative time intervals and uses synchronous switching.

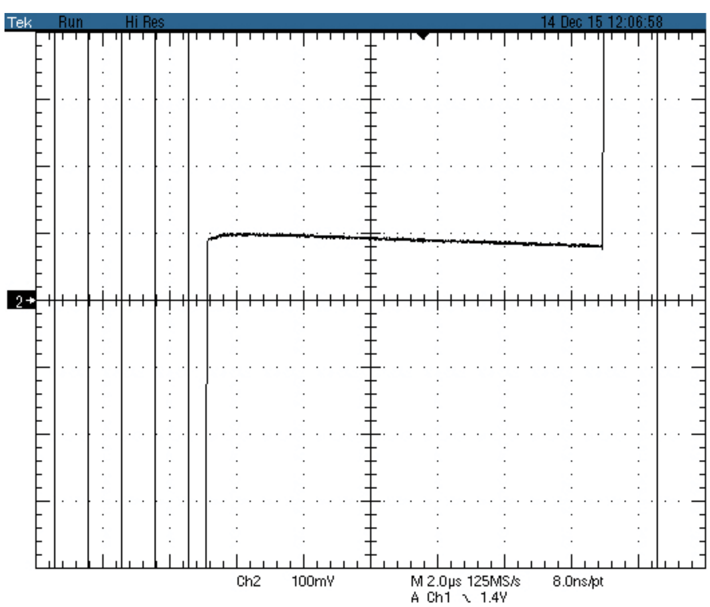
A design may deviate from ideal characteristics when circumstances prevail. Mismatch caused by layout deficiency often results in a consistent tail-off range for each bus, with message-to-message tail-off magnitude changes caused by message length and data differences. Bus A tail-off rarely matches Bus B. Sometimes the contribution from various factors cancels out, moving the tail-off voltage range for that bus closer to zero. Sometimes the various contributions conspire to raise average tail-off magnitude away from zero. Until now, designers had few options other than redesign when unacceptable tail-off occurred. The HI-1585 offers two optional provisions to minimize systemic tail-off occurrence, namely Input Data Synchronization and Bus Tail-off Adjustment. These are both described in the following sections.

FUNCTIONAL DESCRIPTION

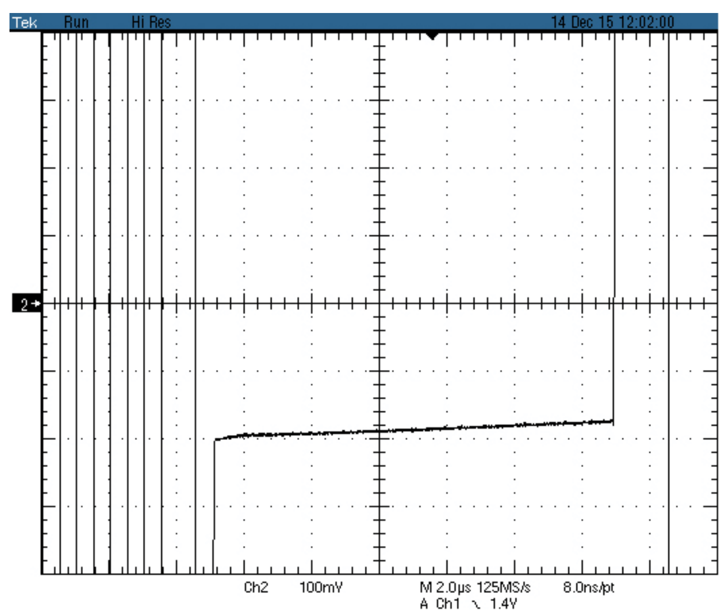




a) Ideal Waveform Has No Tail-off or Ringing



b) Exponentially-Decaying Positive Tail-off



c) Exponentially-Decaying Negative Tail-off

Figure 2. Transmit-induced Tail-off (Offset)

FUNCTIONAL DESCRIPTION

INPUT DATA SYNCHRONIZATION

Timing skew between TX and $\overline{TX}$ is a common cause of MIL-STD-1553 end-of-message offset (tail-off). To accurately align input signal edges, the HI-1585 has latched TX and $\overline{TX}$ inputs. The CLKA and CLKB inputs and the ENCLK configuration pin enable input synchronization for Buses A and B. If using an FPGA encoder, the user must provide a brief positive clock pulse every time the TX and $\overline{TX}$ signals change state. TX and $\overline{TX}$ input data is latched on CLK rising edge. See Figure 1. If ENCLK is held low, the clocked input latches are bypassed; CLKA and CLKB pins are ignored. In this case, accurate TX and $\overline{TX}$ input signal matching is the responsibility of the user.

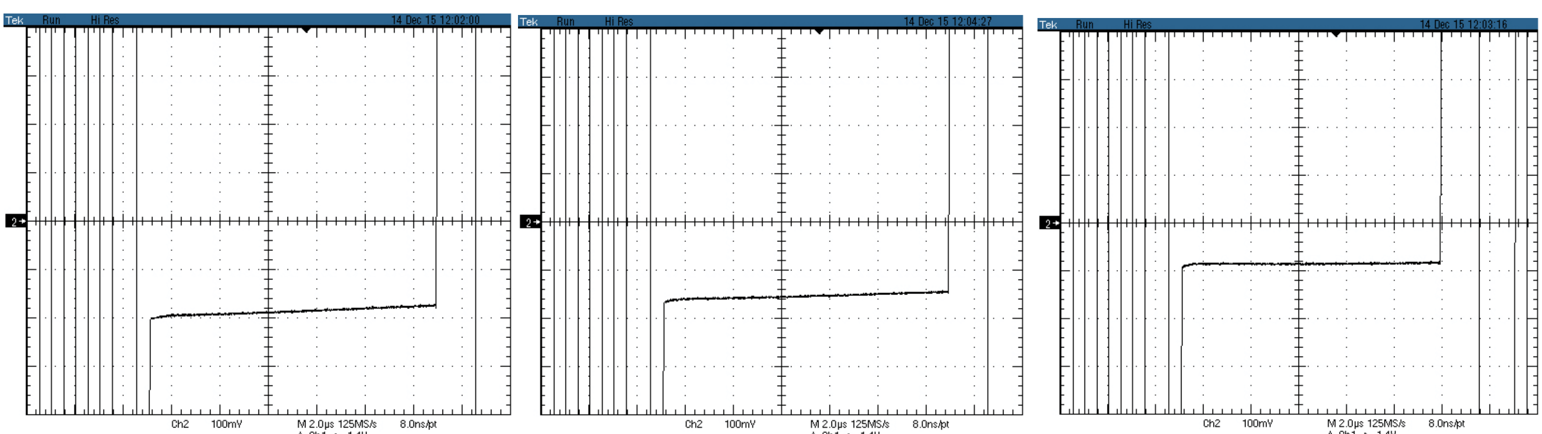
BUS TAIL-OFF ADJUSTMENT

A second provision affecting tail-off performance is output trimming. This method compensates drive characteristics when the HI-1585 drives mismatched signal path impedance between the positive/negative drive output pins and the isolation transformer. Bus A and Bus B each have 3 input pins, TOC[2:0], which present a 3-bit binary argument. Two of the 8 possible states provide zero compensation, and pull-downs force the 3 pins to 0-0-0, a zero compensation state if the TOC pins are left open. Three states provide small-medium-large compensation levels for positive-going tail-off while the three remaining states do the same for negative-going tail-off. Table 2 lists the TOC[2:0] codes and their nominal effect on offset for a transformer-coupled configuration. Figures 3 and 4 illustrate the effect of positive and negative compensation on tail-off. It is envisioned that this would be a one-time setup to compensate for board layout deficiencies that cause consistent tail-off trouble in the same direction. The circuit applies incredibly slight changes to transmitted signal rise time and fall time to achieve compensation. Very slight differences (<1ns) applied to all state changes in a long message have a surprising effect on tail-off level.

NOTE: The compensation values listed below are average values using 32-word messages measured across 6 data patterns (0x0000, 0xFFFF, 0x5555, 0xAAAA, 0x7FFF and 0x8000) in a laboratory test set-up. The applied tail-off shift is proportional to message length. It is recommended that the user evaluate each individual application before applying tail-off compensation.

TOC2	TOC1	TOC0	Tail-off / Offset Shift
0	0	0	0 mV (No correction)
0	0	1	+ 5 mV shift
0	1	0	+ 25mV shift (for negative tail-off)
0	1	1	+75 mV shift
1	0	0	0 mV (No correction)
1	0	1	- 5 mV shift
1	1	0	- 25 mV shift (for positive tail-off)
1	1	1	- 75mV shift

Table 2. TOC[2:0] codes



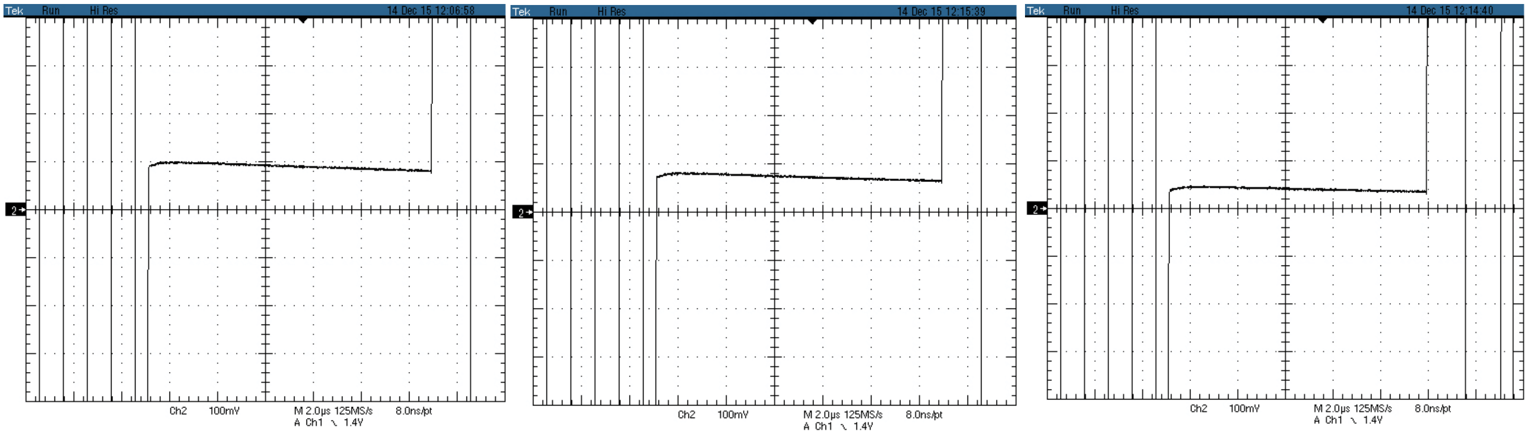
a) Uncompensated, TOC[2:0] = 000 or 100

b) TOC[2:0] = 010

c) TOC[2:0] = 011

Figure 3. Effect of Positive Compensation on Negative Tail-off (Offset)

FUNCTIONAL DESCRIPTION



a) Uncompensated, TOC[2:0] = 000 or 100 b) TOC[2:0] = 110 c) TOC[2:0] = 111

Figure 4. Effect of Negative Compensation on Positive Tail-off (Offset)

RECEIVER

The receiver accepts bi-phase differential analog signals from the MIL-STD-1553 bus through the same direct- or transformer-coupled interface at the BUSAIN and $\overline{\text{BUSAIN}}$ (or BUSBIN and $\overline{\text{BUSBIN}}$) pins. The receiver differential input stage drives a filter and threshold comparator to produce CMOS data at the RXA and $\overline{\text{RXA}}$ (or RXB and $\overline{\text{RXB}}$) output pins. When the MIL-STD-1553 bus is idle and RXENA (or RXENB) receiver enable inputs are high, the corresponding RX and $\overline{\text{RX}}$ output pins will be logic “0”.

Both receiver outputs are forced to the bus idle state (logic “0”) when RXENA or RXENB is low.

RECEIVER OUTPUT PULSE EXTENSION

A unique feature of the HI-1585 is RX and $\overline{\text{RX}}$ output pulse extension. When receiving differential signals near the MIL-STD-1553 minimum amplitude specification (860 mVpp when transformer-coupled), traditional transceivers produce narrow output pulses at RX and $\overline{\text{RX}}$, because the time that analog bus voltage exceeds the receiver threshold is much shorter than for a nominal or large amplitude bus voltage. The HI-1585 receiver pulse outputs can optionally be stretched so that any comparator pulse outputs from RX and $\overline{\text{RX}}$ have a minimum pulse width of 300ns. This function is enabled by strapping the ENPEXT configuration pin high. When ENPEXT is low, the part reverts to traditional operation where RX and $\overline{\text{RX}}$ output pulses reflect just the time that analog bus voltage exceeds comparator threshold voltage.

MIL-STD-1553 BUS INTERFACE

A direct-coupled interface (see Figure 5) uses a 1:2.65 turns-ratio isolation transformer and two 55 ohm isolation resistors between the transformer and the bus. The primary center-tap of the isolation transformer must be connected to GND.

In a transformer-coupled interface (see Figure 5), the transceiver is connected to a 1:2.07 turns-ratio isolation transformer which is connected to the main bus using a 1:1.4 turns-ratio coupling transformer. The transformer coupled method also requires two coupling resistors equal to 75% of the bus characteristic impedance (Zo) between the coupling transformer and the bus.

Figure 6 and Figure 7 show test circuits for measuring electrical characteristics of both direct- and transformer-coupled interfaces respectively. (See electrical characteristics on the following pages).

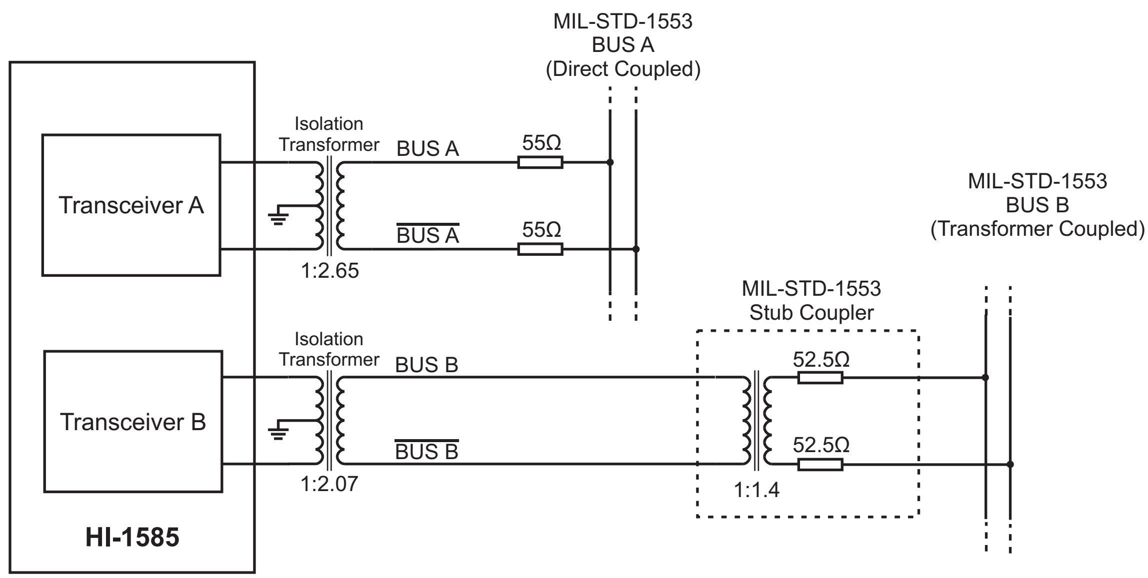
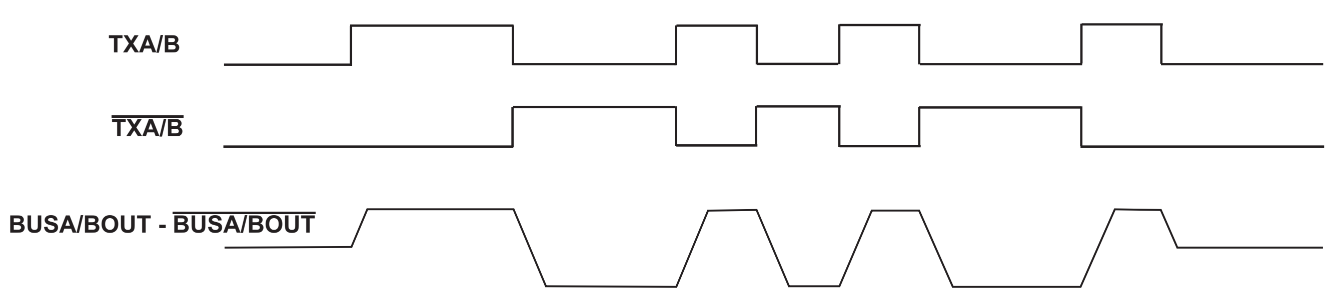
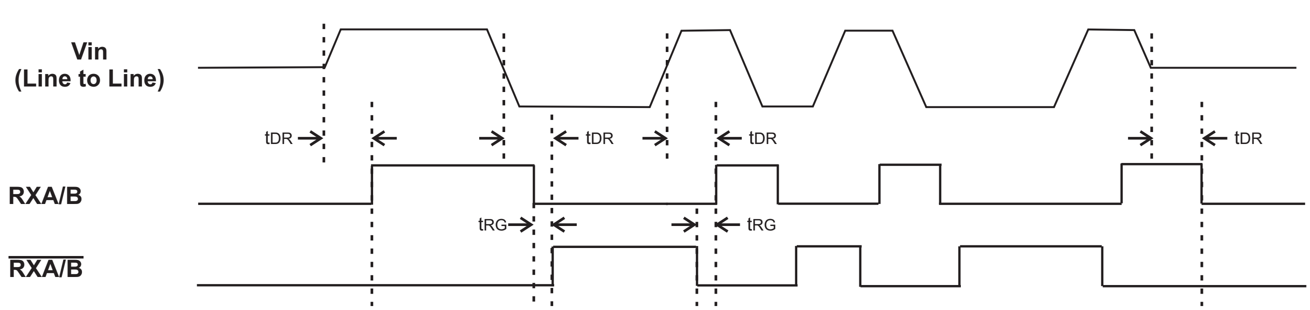


Figure 5. Bus Connection Example

TRANSMIT WAVEFORM - EXAMPLE PATTERN



RECEIVE WAVEFORMS - EXAMPLE PATTERN



ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD})	-0.3 V to +5 V
Logic input voltage range	-0.3 V dc to +3.6 V
Receiver differential voltage	50 Vp-p
Driver peak output current	+1.0 A
Power dissipation at 25°C	1.0 W
Reflow Solder Temperature	260°C
Junction Temperature	175°C
Storage Temperature	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage

V_{DD}...................................... 3.3V... ±5%

Temperature Range

Industrial .... -40°C to +85°C
Hi-Temp .... -55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.14 V to 3.46V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Operating Voltage	V_{DD}		3.14	3.30	3.46	V
Total Supply Current	I_{CC1}	Not Transmitting		30	40	mA
	I_{CC2}	Transmit one bus @ 50% duty cycle		225	320	mA
	I_{CC3}	Transmit one bus @ 100% duty cycle		425	610	mA
Power Dissipation	PD_1	Not Transmitting			0.06	W
	PD_2	Transmit one bus @ 100% duty cycle			0.5	W
Input Voltage (High)	V_{IH}	Digital inputs	70%			V_{DD}
Input Voltage (Low)	V_{IL}	Digital inputs			30%	V_{DD}
Input Current (High)	I_{IH}	RXEN, ENPEXT, ENCLK			20	µA
Pull-Down Current (High)	I_{IHP}	TX, $\overline{TX}$, TXINH, TOC, CLK	20	30	50	µA
Input Current (Low)	I_{IL}	TX, $\overline{TX}$, TXINH, ENCLK, TOC, CLK	-20			µA
Pull-Up Current (Low)	I_{ILP}	RXEN, ENPEXT	-50	-30	-20	µA
Output Voltage (High)	V_{OH}	I_{OUT} = -1.0mA, Digital outputs	90%			V_{DD}
Output Voltage (Low)	V_{IH}	I_{OUT} = 1.0mA, Digital outputs			10%	V_{DD}
RECEIVER (Measured at Point "A_D" in Figure 6 unless otherwise specified)						
Input resistance	R_{IN}	Differential (at chip pins)	5			Kohm
Input capacitance	C_{IN}	Differential			5	pF
Common mode rejection ratio	CMRR		40			dB
Input common mode voltage	V_{ICM}		-10.0		10.0	V-pk
Threshold Voltage - Direct-coupled Detect	V_{THD}	1 MHz Sine Wave Measured at Point "A_D" in Figure 6 RXA/B, $\overline{RXA/B}$ pulse width >70 ns	1.15			Vp-p
No Detect	V_{THND}	No pulse at RXA/B, $\overline{RXA/B}$			0.28	Vp-p
Theshold Voltage - Transformer-coupled Detect	V_{THD}	1 MHz Sine Wave Measured at Point "A_T" in Figure 7 RXA/B, $\overline{RXA/B}$ pulse width >70 ns	0.86			Vp-p
No Detect	V_{THND}	No pulse at RXA/B, $\overline{RXA/B}$			0.20	Vp-p

DC ELECTRICAL CHARACTERISTICS (cont.)

V_{DD} = 3.14 V to 3.46 V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER		SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
TRANSMITTER **(Measured at Point "A_D" in Figure 6 unless otherwise specified)**							
Output Voltage	Direct coupled	V_{OUT}	35 ohm load (Measured at Point "A_D" in Figure 6)	6.0		9.0	Vp-p
	Transformer coupled	V_{OUT}	70 ohm load (Measured at Point "A_T" in Figure 7)	20.0		27.0	Vp-p
Output Noise		V_{ON}	Differential, inhibited			10.0	mVp-p
Output Dynamic Offset Voltage	Direct coupled	V_{DYN}	35 ohm load (Measured at Point "A_D" in Figure 6)	-90		90	mV
	Transformer coupled	V_{DYN}	70 ohm load (Measured at Point "A_T" in Figure 7)	-250		250	mV
Output Capacitance		C_{OUT}	1 MHz sine wave			15	pF

AC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.14 V to 3.46 V, GND = 0V, T_A =Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER **(Measured at Point "A_T" in Figure 7 unless otherwise specified)**						
Receiver Delay	t_{DR}	From input zero crossing to RXA/B or $\overline{RXA/B}$			450	ns
Receiver gap time ENPEXT = 0	t_{RG}	Spacing between RXA/B and $\overline{RXA/B}$ pulses. 1 MHz sine wave applied at point "AT" Figure 7, amplitude range 0.86 Vp-p to 27.0Vp-p	50		365	ns
Receiver gap time ENPEXT = 1	t_{RG}	Spacing between RXA/B and $\overline{RXA/B}$ pulses. 1 MHz sine wave applied at point "AT" Figure 7, amplitude range 0.86 Vp-p to 27.0Vp-p	50		200	ns
Receiver Enable Delay	t_{REN}	From RXENA/B rising or falling edge to RXA/B or $\overline{RXA/B}$			40	ns
TRANSMITTER **(Measured at Point "AT" in Figure 7)**						
Driver Delay	t_{DT}	TXA/B, TXA/B to BUSA/BOUT, BUSA/BOUT			160	ns
Rise time	tr	70 ohm load	100	150	300	ns
Fall Time	tf	70 ohm load	100	150	300	ns
Inhibit Delay	t_{DI-H}	Inhibited output			100	ns
	t_{DI-L}	Active output			150	ns
Tx/$\overline{Tx}$ data set-up time to CLK rising edge	t_{Tx-S}	ENCLK pin enabled (high)	10			ns
Tx/$\overline{Tx}$ data hold time after CLK rising edge	t_{Tx-H}	ENCLK pin enabled (high)	10			ns

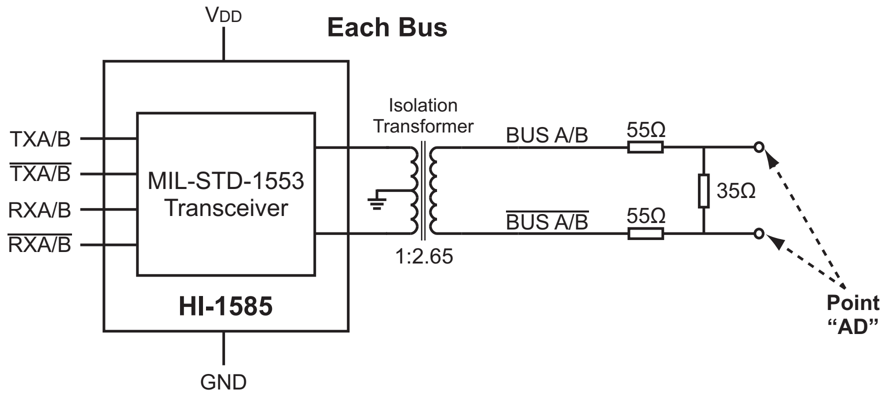


Figure 6. Direct Coupled Test Circuit

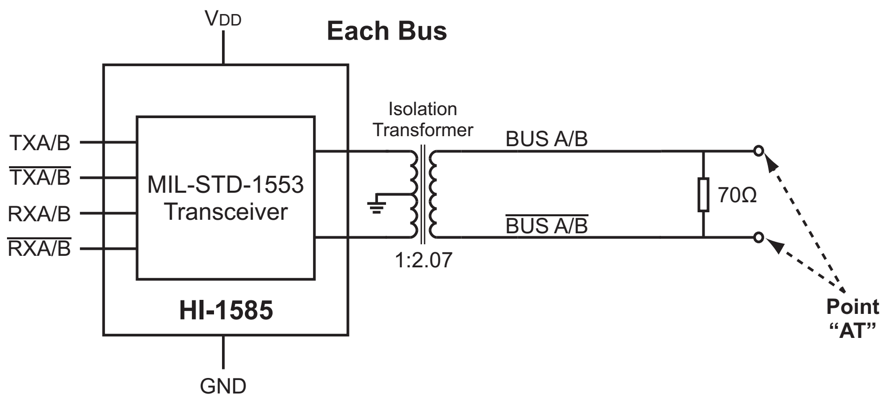


Figure 7. Transformer Coupled Test Circuit

HEAT SINK

The HI-1585PCI/T/M uses a plastic chip-scale package (QFN). These packages include a metal heat sink located on the bottom surface of the device. This heat sink may be soldered down to the printed circuit board for optimum thermal dissipation. The heat sink is electrically isolated and may be soldered to any convenient power or ground plane.

APPLICATIONS NOTE

Holt Applications Note AN-500 provides circuit design notes regarding the use of Holt's family of MIL-STD-1553 transceivers. Layout considerations, as well as recommended interface and protection components are included.

ORDERING INFORMATION

HI - 1585 PC x F

PART NUMBER	LEAD FINISH
F	100% Matte Tin (Pb-free RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No
M	-55°C TO +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION
PC	48 PIN PLASTIC CHIP-SCALE PACKAGE QFN (48PCS6)

RECOMMENDED TRANSFORMERS

The HI-1585 transceiver has been characterized for compliance with the electrical requirements of MIL-STD-1553 when used with the following transformers. Holt recommends Premier Magnetics parts as offering the best combination of electrical performance, low cost and small footprint.

MANUFACTURER	PART NUMBER	APPLICATION	TURNS RATIO	DIMENSIONS
Premier Magnetics	PM-DB2779	Isolation	Dual 1:2.65 / 1:2.07	.675 x .400 x .185 inches
Premier Magnetics	PM-DB2702	Stub coupling	1:1.4	.625 x .625 x .250 inches

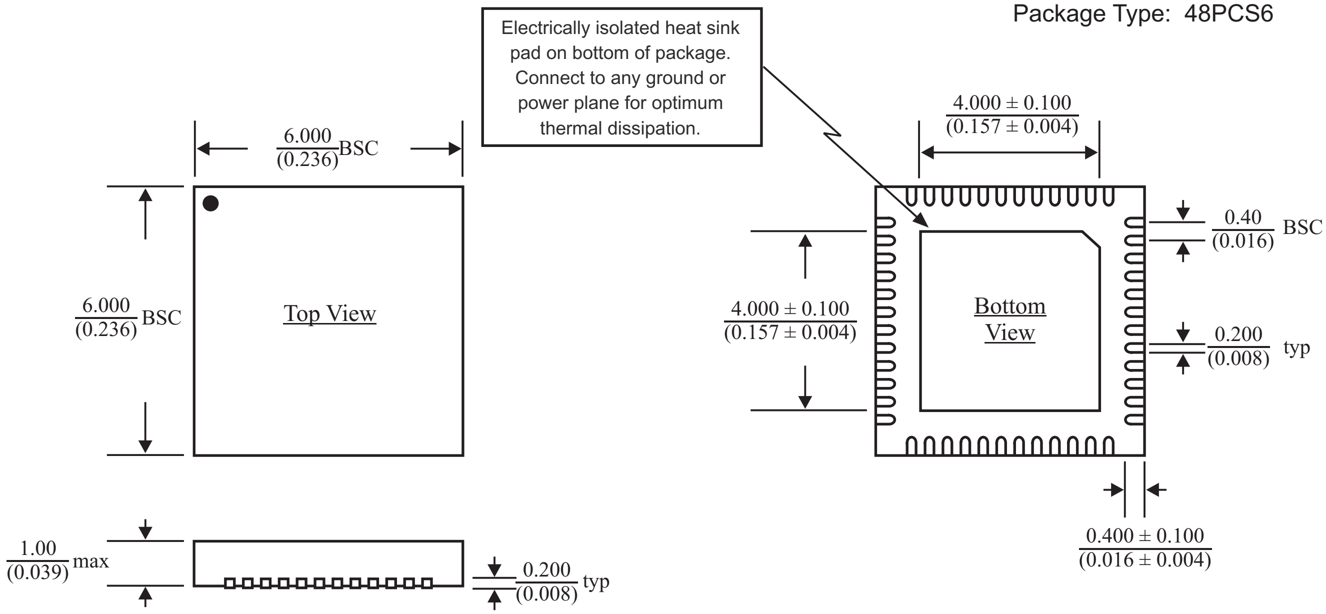
REVISION HISTORY

Document	Rev.	Date	Description of Change
DS1585	New	12/16/15	Initial Release.
	A	02/07/17	Remove Thermal Characteristics Table (refer to web). Update Total Supply Current (Not transmitting) parameter in DC Characteristics Table. Correct other minor typos.
	B	03/02/17	Add Internal pull-down resistors to Pin Descriptions for ENCLKB and ENCLKA pins.

48-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

millimeters (inches)

Package Type: 48PCS6



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)