

April 2015

DESCRIPTION

The HI-8477 is an ARINC 429 Receiver IC, designed for applications where an MCU is not desired or otherwise required. The device does not require an MCU for programmed configuration or operation. It is fully configured using control input pins, greatly simplifying system qualification.

The HI-8477 receives ARINC 429 data directly from the bus and makes the data available at 32 digital output pins. ARINC 429 label filtering is defined by 16 digital input pins, defining a maskable label match to enable reception of a single label or group of labels. A parity check pin provides the user the option of checking for correct odd parity on incoming ARINC 429 words. Incorrect parity words are ignored. If parity checking is turned off, all 32 bits of the ARINC word are stored without parity check.

The HI-8478 performs exactly the same as the HI-8477 with the exception that the 32 digital outputs from the ARINC 429 word are the complement (inverse) of the HI-8477.

The receiver inputs are lightning protected to RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B) with the use of only two external resistors.

A single 1 MHz clock source is required for ARINC 429 bit timing. The device supports both high-speed and low-speed ARINC 429 data rates.

The HI-8477 operates from a single 3.3V or 5.0V power supply.

FEATURES

- Pin programmable - **requires no MCU or software control**
- No need for certification to RTCA DO-178B, "Software Considerations in Airborne Systems and Equipment"
- Robust CMOS Silicon-on-Insulator (SOI) technology
- On-chip ARINC 429 Line Receiver
- 3.3 V or 5V single supply operation
- Maskable Label Filtering for single label or groups of labels
- Internal lightning protection circuitry for receiver inputs allows compliance with RTCA/DO-160G, Section 22 Level 3 Pin Injection Tests using only two external resistors.
- HI-8478 option provides the compliment of HI-8477 digital outputs from the 32-bit ARINC 429 word
- Certifiable to RTCA DO-254, "Design Assurance for Airborne Electronic Hardware"

TYPICAL APPLICATION

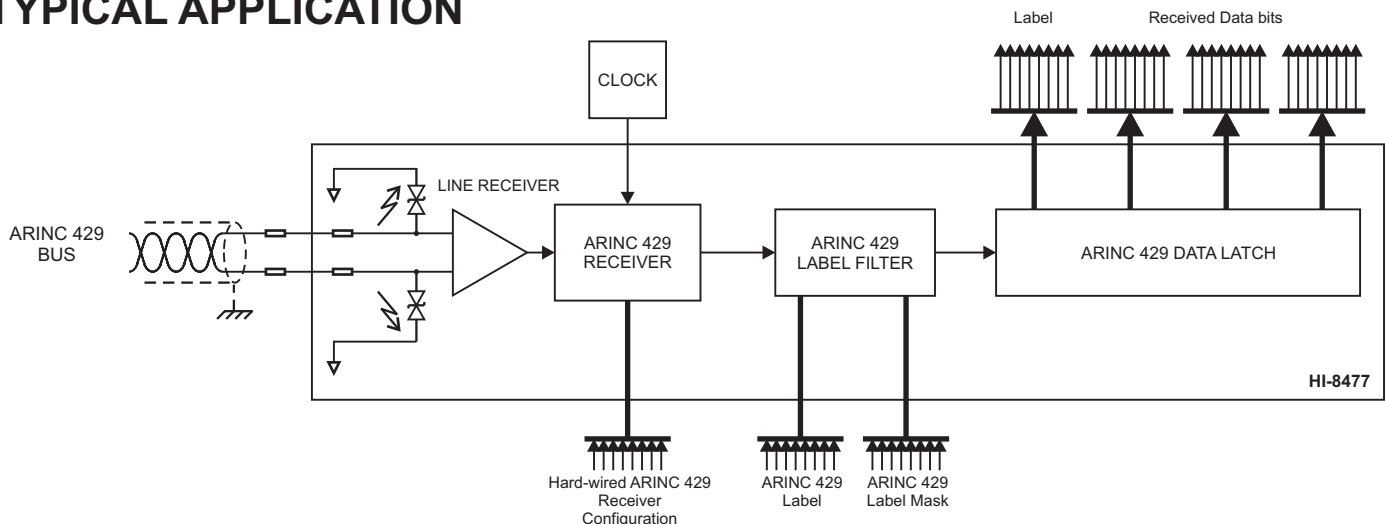


Figure 1

BLOCK DIAGRAM

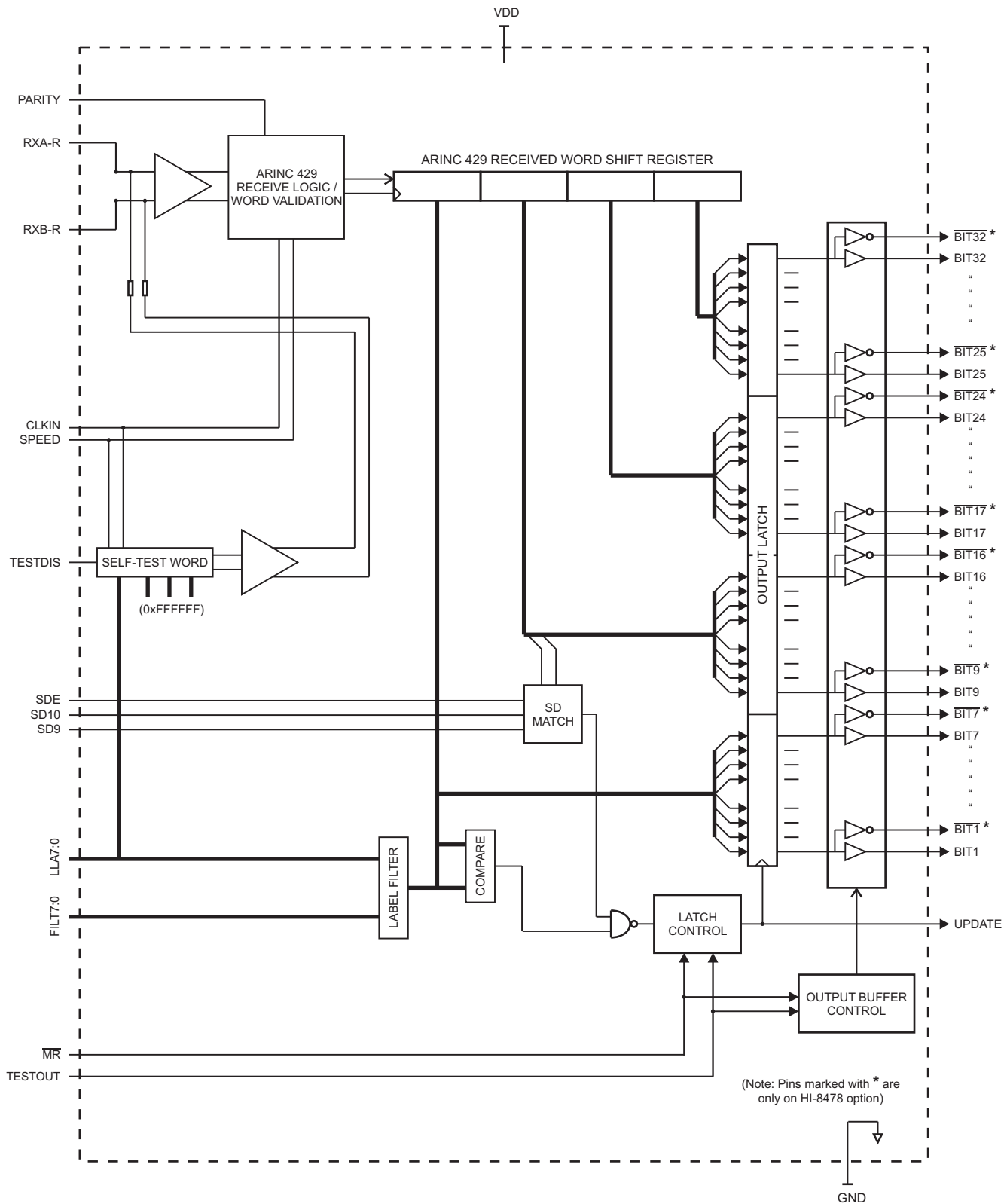


Figure 2

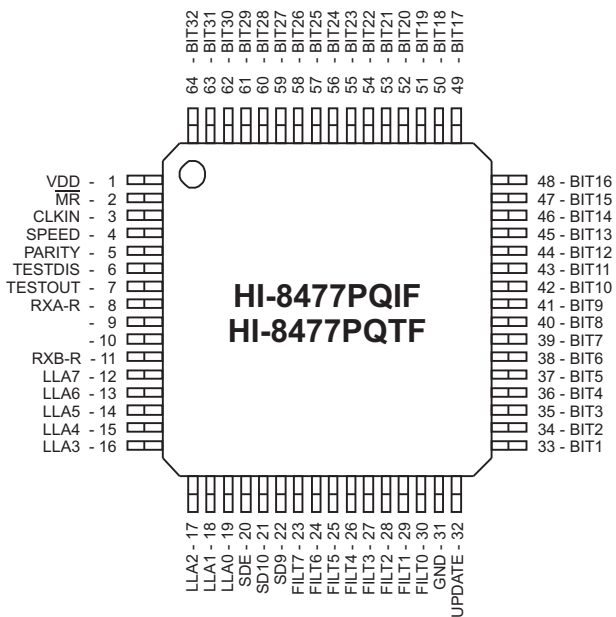
PIN DESCRIPTIONS

| SYMBOL | HI-8477 PIN | HI-8478 PIN | FUNCTION | DESCRIPTION |
|---------------------------|-------------|-------------|----------------|--------------------------------------------------------------------------------------------------------------------------------|
| VDD | 1 | 1 | Supply | 3.3V or 5.0V power |
| $\overline{\text{MR}}$ | 2 | 2 | Digital Input | Master Reset. Active low. Clears the output latch and initializes the ARINC receiver logic |
| CLKIN | 3 | 3 | Digital Input | 1 MHz (+/- 1%) must be provided to operate the ARINC429 receiver |
| SPEED | 4 | 4 | Digital Input | If high ARINC 429 receiver set for 100 kbs, else 12.5 kbs |
| PARITY | 5 | 5 | Digital Input | If high, enables odd parity checking of incoming ARINC 429 words |
| TESTDIS | 6 | 6 | Digital Input | Initiates internal self-test routine following Master Reset when tied low |
| TESTOUT | 7 | 7 | Digital Input | If high, allows self-test word to be output on BIT(1:32) pins at end of self-test routine |
| RXA-R | 8 | 8 | Analog Input | Positive connection to ARINC 429 bus. Used with external 13k Ω resistor. |
| RXB-R | 11 | 11 | Analog Input | Negative connection to ARINC 429 bus. Used with external 13k Ω resistor. |
| LLA7 | 12 | 12 | Digital Input | Label A match bit 7. Compared to ARINC 429 bit 1 when unmasked by FILTER7 |
| LLA6 | 13 | 13 | Digital Input | Label A match bit 6. Compared to ARINC 429 bit 2 when unmasked by FILTER6 |
| LLA5 | 14 | 14 | Digital Input | Label A match bit 5. Compared to ARINC 429 bit 3 when unmasked by FILTER5 |
| LLA4 | 15 | 15 | Digital Input | Label A match bit 4. Compared to ARINC 429 bit 4 when unmasked by FILTER4 |
| LLA3 | 16 | 16 | Digital Input | Label A match bit 3. Compared to ARINC 429 bit 5 when unmasked by FILTER3 |
| LLA2 | 17 | 17 | Digital Input | Label A match bit 2. Compared to ARINC 429 bit 6 when unmasked by FILTER2 |
| LLA1 | 18 | 18 | Digital Input | Label A match bit 1. Compared to ARINC 429 bit 7 when unmasked by FILTER1 |
| LLA0 | 19 | 19 | Digital Input | Label A match bit 0. Compared to ARINC 429 bit 8 when unmasked by FILTER0 |
| SDE | 20 | 20 | Digital Input | When high, ARINC bit 9 and 10 must match SD9 and SD10 for word acceptance |
| SD10 | 21 | 21 | Digital Input | If SDE is high, ARINC bit 9 and 10 must match SD9 and SD10 for word acceptance |
| SD9 | 22 | 22 | Digital Input | If SDE is high, ARINC bit 9 and 10 must match SD9 and SD10 for word acceptance |
| FILTER7 | 23 | 23 | Digital Input | If high, ARINC 429 bit 1 is enabled for label match comparison, else ignore state of ARINC429 bit 1 |
| FILTER6 | 24 | 24 | Digital Input | If high, ARINC 429 bit 2 is enabled for label match comparison, else ignore state of ARINC429 bit 2 |
| FILTER5 | 25 | 25 | Digital Input | If high, ARINC 429 bit 3 is enabled for label match comparison, else ignore state of ARINC429 bit 3 |
| FILTER4 | 26 | 26 | Digital Input | If high, ARINC 429 bit 4 is enabled for label match comparison, else ignore state of ARINC429 bit 4 |
| FILTER3 | 27 | 27 | Digital Input | If high, ARINC 429 bit 5 is enabled for label match comparison, else ignore state of ARINC429 bit 5 |
| FILTER2 | 28 | 28 | Digital Input | If high, ARINC 429 bit 6 is enabled for label match comparison, else ignore state of ARINC429 bit 6 |
| FILTER1 | 29 | 29 | Digital Input | If high, ARINC 429 bit 7 is enabled for label match comparison, else ignore state of ARINC429 bit 7 |
| FILTER0 | 30 | 30 | Digital Input | If high, ARINC 429 bit 8 is enabled for label match comparison, else ignore state of ARINC429 bit 8 |
| GND | 31 | 31 | Supply | 0V supply pin |
| UPDATE | 32 | 32 | Digital Output | Transitions high when a new word is transferred to the output latch and remains high until the next (new) word is transferred. |
| $\overline{\text{BIT1}}$ | N/A | 33 | Digital Output | ARINC 429 bit 1 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT1 | 33 | N/A | Digital Output | ARINC 429 bit 1 output from qualified received word, updated on UPDATE rising edge |
| $\overline{\text{BIT2}}$ | N/A | 34 | Digital Output | ARINC 429 bit 2 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT2 | 34 | N/A | Digital Output | ARINC 429 bit 2 output from qualified received word, updated on UPDATE rising edge |
| $\overline{\text{BIT3}}$ | N/A | 35 | Digital Output | ARINC 429 bit 3 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT3 | 35 | N/A | Digital Output | ARINC 429 bit 3 output from qualified received word, updated on UPDATE rising edge |
| $\overline{\text{BIT4}}$ | N/A | 36 | Digital Output | ARINC 429 bit 4 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT4 | 36 | N/A | Digital Output | ARINC 429 bit 4 output from qualified received word, updated on UPDATE rising edge |
| $\overline{\text{BIT5}}$ | N/A | 37 | Digital Output | ARINC 429 bit 5 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT5 | 37 | N/A | Digital Output | ARINC 429 bit 5 output from qualified received word, updated on UPDATE rising edge |
| $\overline{\text{BIT6}}$ | N/A | 38 | Digital Output | ARINC 429 bit 6 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT6 | 38 | N/A | Digital Output | ARINC 429 bit 6 output from qualified received word, updated on UPDATE rising edge |
| $\overline{\text{BIT7}}$ | N/A | 39 | Digital Output | ARINC 429 bit 7 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT7 | 39 | N/A | Digital Output | ARINC 429 bit 7 output from qualified received word, updated on UPDATE rising edge |
| $\overline{\text{BIT8}}$ | N/A | 40 | Digital Output | ARINC 429 bit 8 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT8 | 40 | N/A | Digital Output | ARINC 429 bit 8 output from qualified received word, updated on UPDATE rising edge |
| $\overline{\text{BIT9}}$ | N/A | 41 | Digital Output | ARINC 429 bit 9 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT9 | 41 | N/A | Digital Output | ARINC 429 bit 9 output from qualified received word, updated on UPDATE rising edge |
| $\overline{\text{BIT10}}$ | N/A | 42 | Digital Output | ARINC 429 bit 10 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT10 | 42 | N/A | Digital Output | ARINC 429 bit 10 output from qualified received word, updated on UPDATE rising edge |

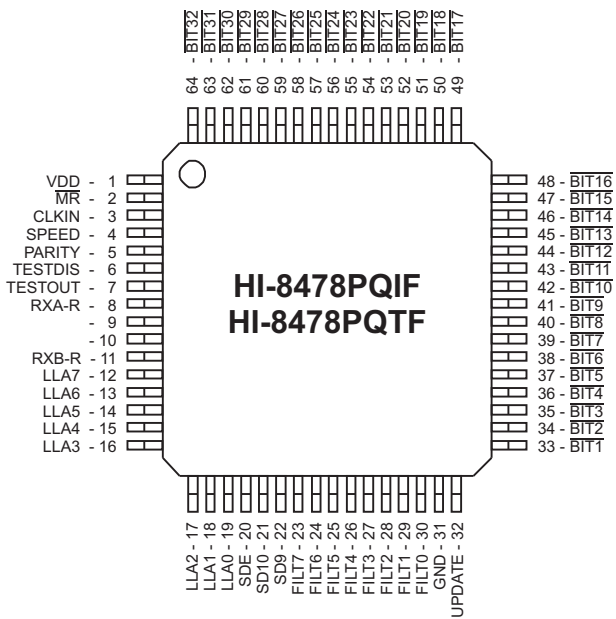
PIN DESCRIPTIONS (cont.)

| SYMBOL | HI-8477 PIN | HI-8478 PIN | FUNCTION | DESCRIPTION |
|--------|----------------|----------------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BIT11 | N/A | 43 | Digital Output | ARINC 429 bit 11 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT11 | 43 | N/A | Digital Output | ARINC 429 bit 11 output from qualified received word, updated on UPDATE rising edge |
| BIT12 | N/A | 44 | Digital Output | ARINC 429 bit 12 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT12 | 44 | N/A | Digital Output | ARINC 429 bit 12 output from qualified received word, updated on UPDATE rising edge |
| BIT13 | N/A | 45 | Digital Output | ARINC 429 bit 13 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT13 | 45 | N/A | Digital Output | ARINC 429 bit 13 output from qualified received word, updated on UPDATE rising edge |
| BIT14 | N/A | 46 | Digital Output | ARINC 429 bit 14 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT14 | 46 | N/A | Digital Output | ARINC 429 bit 14 output from qualified received word, updated on UPDATE rising edge |
| BIT15 | N/A | 47 | Digital Output | ARINC 429 bit 15 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT15 | 47 | N/A | Digital Output | ARINC 429 bit 15 output from qualified received word, updated on UPDATE rising edge |
| BIT16 | N/A | 48 | Digital Output | ARINC 429 bit 16 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT16 | 48 | N/A | Digital Output | ARINC 429 bit 16 output from qualified received word, updated on UPDATE rising edge |
| BIT17 | N/A | 49 | Digital Output | ARINC 429 bit 17 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT17 | 49 | N/A | Digital Output | ARINC 429 bit 17 output from qualified received word, updated on UPDATE rising edge |
| BIT18 | N/A | 50 | Digital Output | ARINC 429 bit 18 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT18 | 50 | N/A | Digital Output | ARINC 429 bit 18 output from qualified received word, updated on UPDATE rising edge |
| BIT19 | N/A | 51 | Digital Output | ARINC 429 bit 19 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT19 | 51 | N/A | Digital Output | ARINC 429 bit 19 output from qualified received word, updated on UPDATE rising edge |
| BIT20 | N/A | 52 | Digital Output | ARINC 429 bit 20 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT20 | 52 | N/A | Digital Output | ARINC 429 bit 20 output from qualified received word, updated on UPDATE rising edge |
| BIT21 | N/A | 53 | Digital Output | ARINC 429 bit 21 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT21 | 53 | N/A | Digital Output | ARINC 429 bit 21 output from qualified received word, updated on UPDATE rising edge |
| BIT22 | N/A | 54 | Digital Output | ARINC 429 bit 22 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT22 | 54 | N/A | Digital Output | ARINC 429 bit 22 output from qualified received word, updated on UPDATE rising edge |
| BIT23 | N/A | 55 | Digital Output | ARINC 429 bit 23 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT23 | 55 | N/A | Digital Output | ARINC 429 bit 23 output from qualified received word, updated on UPDATE rising edge |
| BIT24 | N/A | 56 | Digital Output | ARINC 429 bit 24 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT24 | 56 | N/A | Digital Output | ARINC 429 bit 24 output from qualified received word, updated on UPDATE rising edge |
| BIT25 | N/A | 57 | Digital Output | ARINC 429 bit 25 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT25 | 57 | N/A | Digital Output | ARINC 429 bit 25 output from qualified received word, updated on UPDATE rising edge |
| BIT26 | N/A | 58 | Digital Output | ARINC 429 bit 26 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT26 | 58 | N/A | Digital Output | ARINC 429 bit 26 output from qualified received word, updated on UPDATE rising edge |
| BIT27 | N/A | 59 | Digital Output | ARINC 429 bit 27 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT27 | 59 | N/A | Digital Output | ARINC 429 bit 27 output from qualified received word, updated on UPDATE rising edge |
| BIT28 | N/A | 60 | Digital Output | ARINC 429 bit 28 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT28 | 60 | N/A | Digital Output | ARINC 429 bit 28 output from qualified received word, updated on UPDATE rising edge |
| BIT29 | N/A | 61 | Digital Output | ARINC 429 bit 29 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT29 | 61 | N/A | Digital Output | ARINC 429 bit 29 output from qualified received word, updated on UPDATE rising edge |
| BIT30 | N/A | 62 | Digital Output | ARINC 429 bit 30 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT30 | 62 | N/A | Digital Output | ARINC 429 bit 30 output from qualified received word, updated on UPDATE rising edge |
| BIT31 | N/A | 63 | Digital Output | ARINC 429 bit 31 inverted output from qualified received word, updated on UPDATE rising edge |
| BIT31 | 63 | N/A | Digital Output | ARINC 429 bit 31 output from qualified received word, updated on UPDATE rising edge |
| BIT32 | N/A | 64 | Digital Output | BIT32 inverted output. |
| BIT32 | 64 | N/A | Digital Output | ARINC 429 bit 32 output from qualified received word, updated on UPDATE rising edge. If PARITY pin is HIGH, parity checking is enabled. Received words with incorrect parity are ignored. |

PIN CONFIGURATIONS



64-pin Plastic Quad Flatpack (PQFP)



64-pin Plastic Quad Flatpack (PQFP)

Figure 3

FUNCTIONAL DESCRIPTION

OVERVIEW

The HI-8477 and HI-8478 are autonomous ARINC 429 receivers intended for applications where a host MCU is either undesirable or not otherwise needed. The parts contain an on-chip ARINC 429 line receiver and protocol logic to decode and capture selected ARINC 429 data words. The ARINC 429 word is made available to the application on 32 CMOS output pins, which may be used to directly control subsystem functions. The HI-8478 device provides data which is the complement of HI-8477.

ARINC 429 LINE RECEIVER

An on-chip ARINC 429 analog receiver operates from the same supply as the digital logic. Two input pins, RXA-R and RXB-R, require an external series resistor of 13 kOhm between the pin and ARINC 429 bus for proper signal level detection. With these resistors the inputs are lightning protected to RTCA/DO-160G, Section 22 Level 3 Pin Injection, Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B).

Application Note AN-301 provides guidelines for enhanced lightning protection circuitry.

RESET OPERATION

Applications may wire the device outputs directly to logic, relay drivers, DACs, etc. It is therefore important to define the state of the outputs during the interval between system reset and the reception of a first, valid ARINC 429 word.

The HI-8477 holds all BIT1:32 outputs in tri-state following reset. The pins have internal weak (60kOhm) pull-down resistors. This provision allows hardwiring 10kOhm resistors at each output to VDD or GND to set the initial state of the 32 bits. The HI-8478 does not have this feature; all BIT1:32 outputs will be logic "High" following reset.

ARINC 429 WORD DECODER

A 1MHz clock at CLKIN samples the outputs of the ARINC 429 receiver at ten times the nominal bit rate. The SPEED pin should be set to a zero when connecting the HI-8477 to a low-speed (12.5kb/s) ARINC 429 bus, or to a one for connection to a high-speed (100kb/s) bus. The PARITY pin selects whether parity checking of incoming ARINC 429 words is enabled. If the PARITY pin is set high, the receiver logic checks for odd parity. If odd parity was received, the word is stored unaltered in the input shift register (see Figure 2). **If even parity was received (error), the word is discarded.** Setting the PARITY pin low disables parity checking and all ARINC 429 received words are passed to the input shift register unaltered.

LABEL FILTERING

All properly encoded ARINC 429 received data words are captured by the input shift register. However, only words meeting user-specified label and SD values are then passed to the output latch (see Figure 2). Eight label match inputs, LLA:(7:0), and eight filter inputs, FILT(7:0) define the label match criteria. Setting a filter bit high enables matching for that bit of the received ARINC 429 label byte. If FILTn is high, the ARINC label bit must match the value at LLAn for the word to be accepted. Setting FILTn low, disables matching for that bit, declaring it a "don't care" bit.

Setting FILT(7:0) to 0x00 turns off label matching for all label bits; in this case the HI-8477 accepts all ARINC 429 labels. Judicious selection of LLA(7:0) and FILT(7:0) values allows either a single ARINC 429 label to be accepted by the filter or a group of labels. For example, setting FILT(7:0) to 0xFC and LLA(7:0) to 0x80, accepts ARINC 429 labels 0x80 through 0x83 only (10 - 13 octal).

Note that ARINC 429 defines the label bits as "big-endian". Therefore received ARINC 429 bit 1 is the MSB (label bit 7), and ARINC received bit 8 is the LSB (label bit 0). Thus LLA7 and FILT7 compare ARINC bit 1, LLA6 and FILT6 compare ARINC bit 2, etc.

ARINC bits 9 and 10 are the SD bits. Incoming ARINC 429 words captured in the input shift register may also be compared for SD matching as a condition for passing to the output latch. Taking the SDE pin high enables this feature. When SDE is high, ARINC bits 9 and 10 are compared with the state of the SD9 and SD10 input pins. Label filtering AND SDE matching criteria must be met to allow a received word to be passed to the output latch.

PARALLEL OUTPUT DATA

Data is passed to the output latch one CLKIN period before the rising edge of the UPDATE pin and remains stable until a new valid and label-matching ARINC 429 word is received. UPDATE goes low as soon as the first bit of a potential new ARINC 429 word is detected by the receiver.

FUNCTIONAL DESCRIPTION (cont.)

SELF-TEST OPERATION

The HI-8477 includes a self-test feature. See Figure 2. The purpose of the Self-Test word block is to send a test transmission to the Receiver inputs (after the input resistor) coded with LLA followed by all Ones. It is activated by an edge sensitive input. The edge is generated on the first clock (CLKIN pin) after the Master Reset rising edge, only if the TESTDIS input is wired Low. The user has the option of enabling the received self-test word to be latched into the output latch and made available at the BIT(1:32) outputs. If the TESTOUT input is high, the tri-state operation after Master Reset is cancelled one CLKIN period before UPDATE goes high and the test word is output at BIT(1:32). If TESTOUT is low, the BIT(1:32) outputs remain in tri-state until the first valid and matching ARINC 429 word is received. The UPDATE pin stays high until the first bit of a potential new ARINC 429 word is received.

Note that label and SDE filtering apply equally to the self-test word as for normal operation.

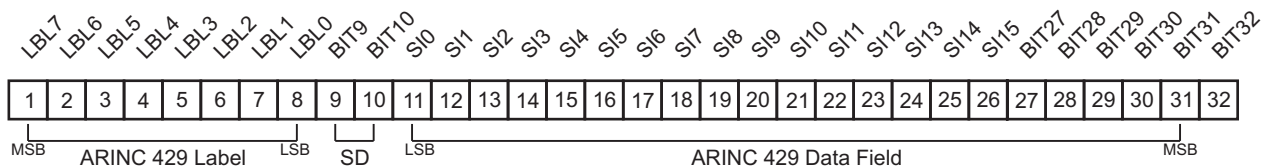


Figure 4. ARINC 429 Word Format

LIGHTNING PROTECTION

The ARINC 429 data bus inputs, RXA and RXB, are lightning protected to RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B) with the use of 13kOhm external resistors. See application notes AN-300 and AN-301 for further details on lightning protection. Figures 5, 6 and 7 summarize the waveforms.

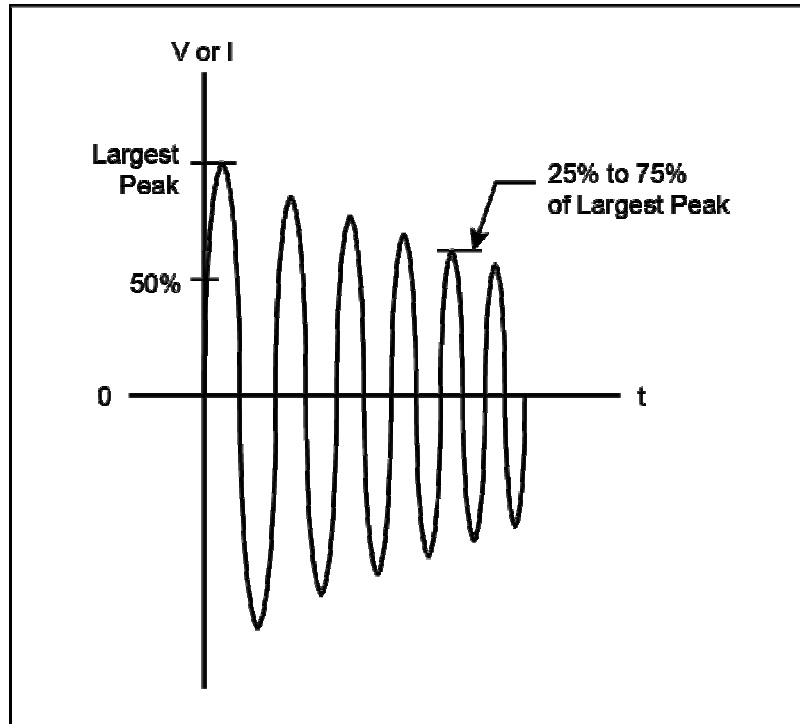


Figure 5. DO-160G Lightning Induced Transient Voltage Waveform 3.
 $V_{oc} = 600V$, $I_{sc} = 24A$, Frequency = $1MHz \pm 20\%$.

Waveform 4

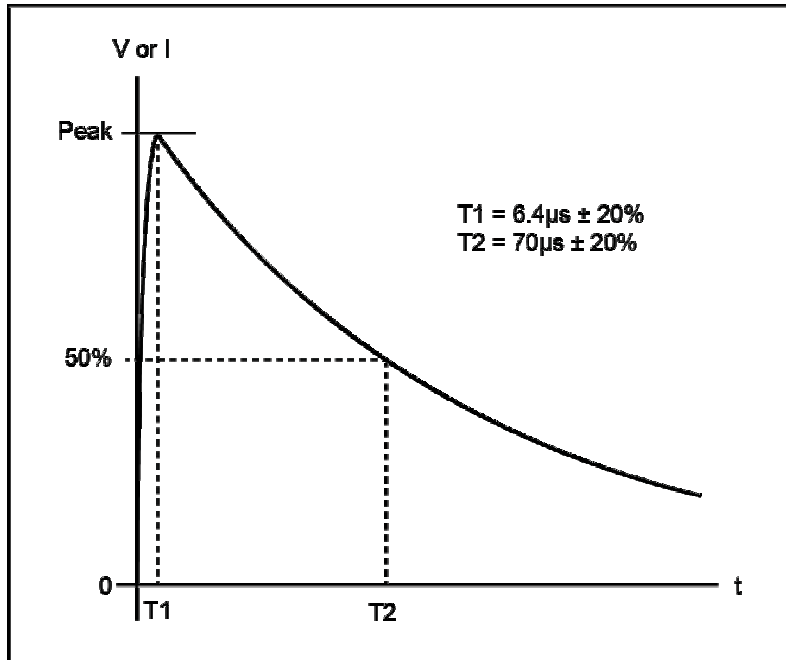


Figure 6. DO-160G Lightning Induced Transient Voltage Waveform 4.
 $V_{oc} = 300V$, $I_{sc} = 60A$.

Waveform 5

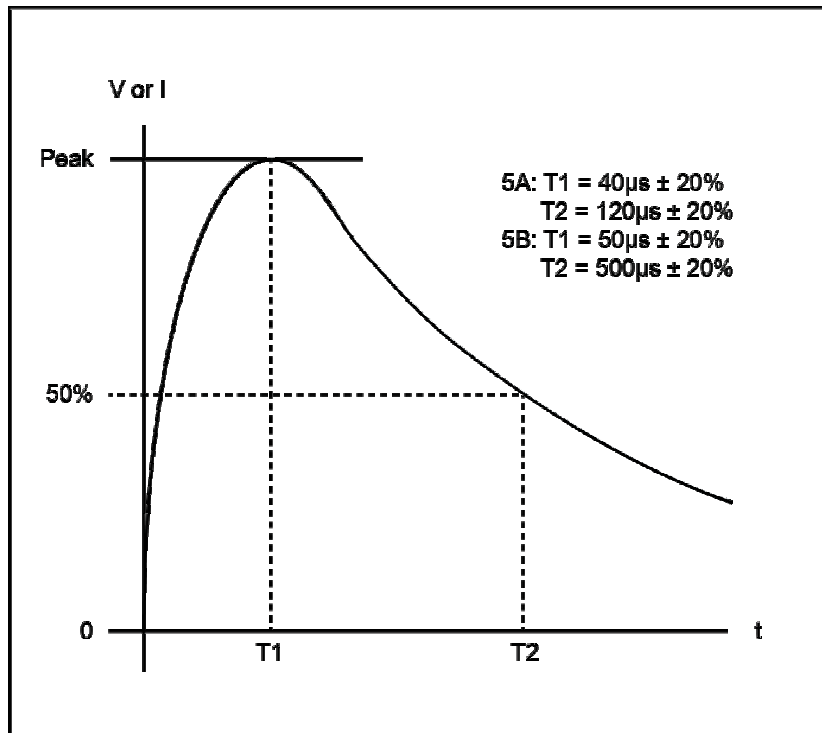


Figure 6. DO-160G Lightning Induced Transient Voltage Waveforms 5A and 5B.
 $V_{oc} = 300V$, $I_{sc} = 300A$.

ABSOLUTE MAXIMUM RATINGS

| | |
|---------------------------------------------------------------------------------|----------------------|
| Voltages referenced to Ground | |
| Supply Voltage (VDD) | -0.3V to +7V |
| Maximum Current at any pin | -150 mA |
| Logic Input Voltage Range | -0.3V to VLOGIC+0.3V |
| ARINC 429 Input Voltage Range | -120V to +120V |
| Continuous Power Dissipation (TA=+70°C) (derate 10.0mW/°C above +70°C) | 1.5W |
| Solder Temperature (reflow) | 260°C |
| Junction Temperature | 175°C |
| Storage Temperature | -65°C to +150°C |

RECOMMENDED OPERATING CONDITIONS

| | |
|-----------------------------|-----------------|
| Supply Voltage | |
| VLOGIC | 3.0V to 5.5V |
| Operating Temperature Range | |
| Industrial Screening | -40°C to +85°C |
| Hi-Temp Screening | -55°C to +125°C |

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

D.C. ELECTRICAL CHARACTERISTICS

VDD = 3.0 to 5.5V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|-------------------------------------------------------------------------------------|---------------------|---------------------------------------|-------|-----|-------|-------|
| ARINC 429 RECEIVER INPUTS (RXA-R/RXB-R with external 13 kΩ series resistors) | | | | | | |
| ARINC input voltage | | | | | | |
| one or zero | V _{DIN} | Differential voltage | 6.5 | 10 | | V |
| null | V _{NIN} | " " " | - | - | 2.5 | V |
| common mode | V _{COM} | with respect to ground | -30.0 | - | +30.0 | V |
| ARINC input resistance | | | | | | |
| RINA-R to RINB-R | R _{DIFF} | Supplies floating | - | 200 | - | kΩ |
| RINA-R or RINB-R to GND | R _{GND} | " " | - | 140 | - | kΩ |
| RINA-R or RINB-R to VCC | R _{VCC} | " " | - | 100 | - | kΩ |
| LOGIC INPUTS | | | | | | |
| Input Voltage | V _{IH} | Input Voltage HI | 70% | | | VDD |
| | V _{IL} | Input Voltage LO | | | 30% | VDD |
| Input Current | I _{SINK} | V _{IN} = VDD | | | 1 | μA |
| | I _{SOURCE} | V _{IN} = GND | -1 | | | μA |
| LOGIC OUTPUTS | | | | | | |
| Output Voltage | V _{OH} | I _{OH} = -100μA | 90% | | | VDD |
| | V _{OL} | I _{OL} = 100μA | | | 10% | VDD |
| Output Current | I _{OL} | V _{OUT} = 0.4V | 1.6 | | | mA |
| | I _{OH} | V _{OUT} = VLOGIC - 0.4V | | | -1.0 | mA |
| Tri-state Current (HI-8477, BIT1 - BIT32 only) | I _{OZH} | V _{IN} = VDD, 60kΩ pull down | 20 | 50 | 80 | μA |
| | I _{OZL} | V _{IN} = GND | -1 | | | μA |

D.C. ELECTRICAL CHARACTERISTICS (cont.)

VDD = 3.0 to 5.5V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

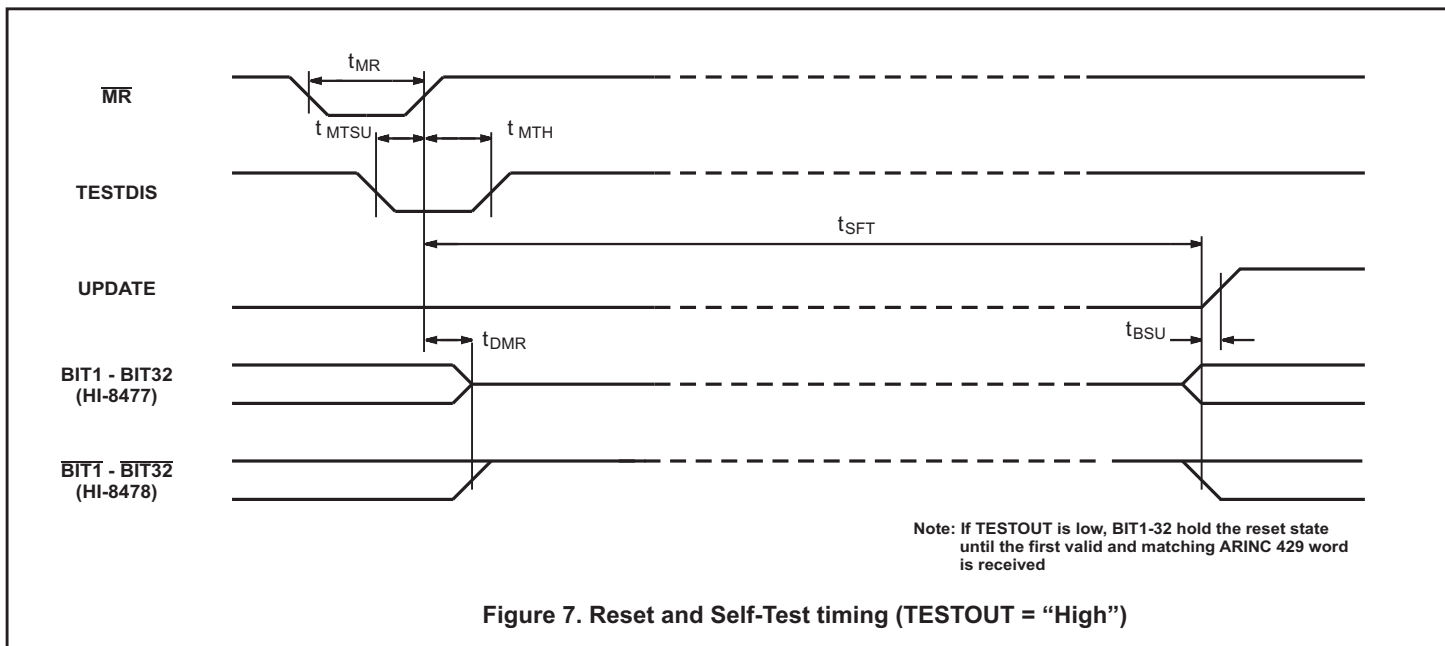
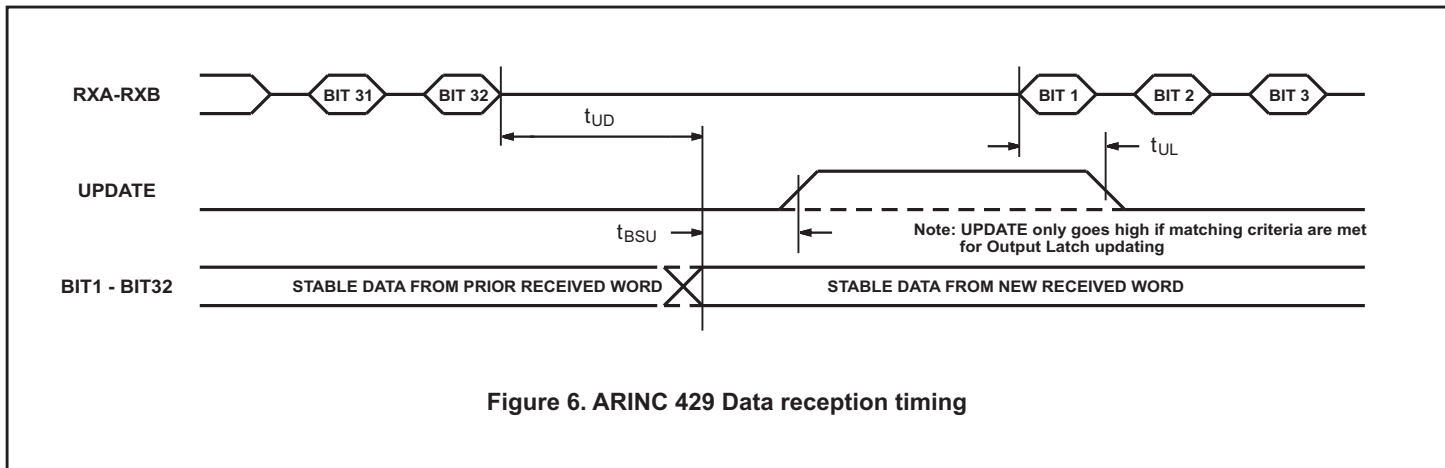
| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|--------------------|------------------|------------------------|-----|-----|-----|-------|
| SUPPLY | | | | | | |
| VDD Supply current | I _{DD5} | V _{DD} = 5.5V | | 5 | 8 | mA |
| | I _{DD3} | V _{DD} = 3.6V | | 4 | 6 | mA |
| CAPACITANCE | | | | | | |
| Output Capacitance | C _O | | | 15 | | pF |
| Output Capacitance | C _I | | | 5 | | pF |

AC ELECTRICAL CHARACTERISTICS

VDD = 3.0 to 5.5V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

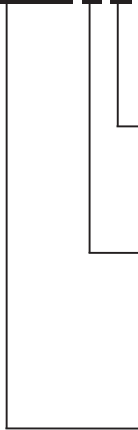
| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|-----------------------------------------------------|--------------------|-----------------------------------------------------------|--------|-----|---------|-------|
| CLOCK | | | | | | |
| CLKIN Frequency | f _{CLK} | | 0.99 | | 1.01 | MHZ |
| CLKIN Mark : Space Ratio | t _{CLKMS} | | 40 | | 60 | % |
| DATA RECEPTION | | | | | | |
| Delay, ARINC 429 word received to BIT1-32 change | t _{UD} | SPEED = 1 (100kb/s ARINC 429) | | | 10 | μs |
| | t _{UD} | SPEED = 0 (12.5kb/s ARINC 429) | | | 80 | μs |
| Delay ARINC bit 1 to UPDATE low | t _{UL} | SPEED = 1 (100kb/s ARINC 429) | | | 10 | μs |
| | t _{UL} | SPEED = 0 (12.5kb/s ARINC 429) | | | 80 | μs |
| BIT1-32 change before UPDATE high | t _{BSU} | D = 1/CLKIN for High speed D = 8/(CLKIN) for Low speed | D - 50 | D | D + 150 | ns |
| RESET & SELF TEST | | | | | | |
| Master Reset (\overline{MR}) Pulse width | t _{MR} | | 100 | | | ns |
| TESTDIS to \overline{MR} rising edge set-up time | t _{MTSU} | | 50 | | | ns |
| TESTDIS after \overline{MR} rising edge hold time | t _{MTH} | | 50 | | | ns |
| Self-test execution time | t _{SFT} | SPEED = 1 (100kb/s ARINC 429) | | | 400 | μs |
| | t _{SFT} | SPEED = 0 (12.5kb/s ARINC 429) | | | 3 | ms |
| Delay MR rising to BIT default state | t _{DMR} | | | | 50 | ns |
| | | | | | | |

TIMING DIAGRAMS



ORDERING INFORMATION

HI - 847xPQ x F



| PART NUMBER | LEAD FINISH |
|-------------|------------------------------------------|
| F | 100% Matte Tin (Pb-free, RoHS compliant) |

| PART NUMBER | TEMPERATURE RANGE | FLOW | BURN IN |
|-------------|-------------------|------|---------|
| I | -40°C TO +85°C | I | NO |
| T | -55°C TO +125°C | T | NO |

| PART NUMBER | PACKAGE DESCRIPTION |
|-------------|--------------------------------------|
| 8477PQ | 64 PIN PLASTIC QUAD FLATPACK (64PQS) |
| 8478PQ | 64 PIN PLASTIC QUAD FLATPACK (64PQS) |

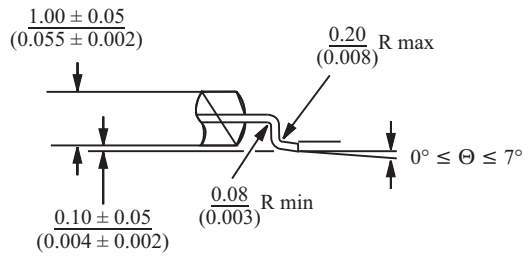
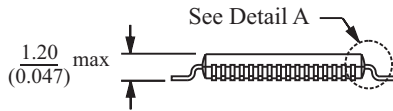
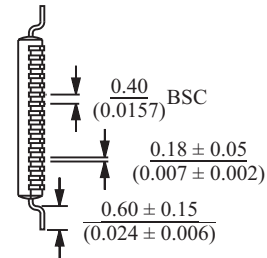
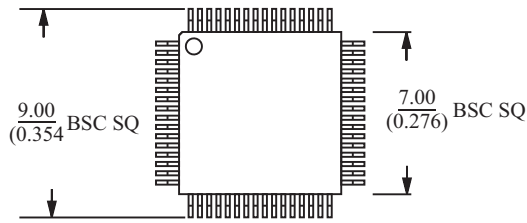
REVISION HISTORY

| P/N | Rev | Date | Description of Change |
|--------|-----|----------|-----------------------|
| DS8477 | New | 04/01/15 | Initial Release |

64 PIN PLASTIC THIN QUAD FLAT PACK (TQFP)

millimeters (inches)

Package Type: 64PQS



Detail A

BSC = "Basic Spacing between Centers"
is theoretical true position dimension and
has no tolerance. (JEDEC Standard 95)