HOLT INTEGRATED CIRCUITS INC.

HI-1575

April 2011

MIL-STD-1553 3.3V Dual Transceivers with Integrated Encoder / Decoders

DESCRIPTION

The HI-1575 is a low power CMOS dual transceiver with on-chip Manchester II Encoder and dual Decoder designed to meet the requirements of the MIL-STD-1553 specification. The part acts as a "Smart Transceiver", allowing users to transmit and receive properly encoded MIL-STD-1553 Command and Data words between a 16-bit host processor and dual MIL-STD-1553 data buses.

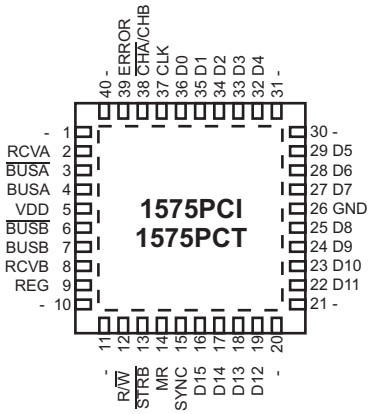
A single write cycle is used to transfer a word to the HI-1575, which encodes the data, adds the selected Sync and Parity bits, and transmits the word on the chosen MIL-STD-1553 data bus. Complete MIL-STD-1553 messages may be transmitted by executing multiple write cycles to the device.

Activity on both MIL-STD-1553 data buses is continuously monitored. When the HI-1575 detects a properly encoded word, a hardware interrupt is generated and the information is decoded and stored in one of two internal registers, which may then be read by the host processor. Bits in the internal Status & Mode Register indicate on which bus the word was received and whether the word had a Data or Command Sync.

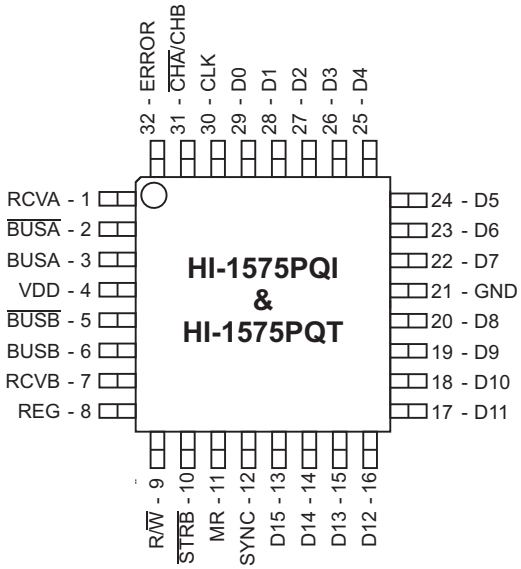
FEATURES

- Compliant to MIL-STD-1553A & B
- 3.3V single supply operation
- On-chip Encoder and Dual Decoder
- Small footprint available in 32-pin plastic TQFP package
- Less than 0.5W maximum power dissipation
- 6 mm x 6 mm 40-pin plastic chip-scale package option

PIN CONFIGURATIONS



40 Pin Plastic 6mm x 6mm Chip-scale package



32 Pin TQFP package

PIN DESCRIPTIONS

PIN (TQFP)	SYMBOL	FUNCTION	PULL-UP PULL-DOWN	DESCRIPTION
1	RCVA	Digital output	-	Goes high when MIL-STD-1553 word received on Bus A
2	$\overline{\text{BUSA}}$	Analog I/O	-	MIL-STD-1533 bus driver A, negative signal
3	BUSA	Analog I/O	-	MIL-STD-1553 bus driver A, positive signal
4	VDD	Power supply	-	+3.3 VDC
5,	$\overline{\text{BUSB}}$	Analog I/O	-	MIL-STD-1533 bus driver B, negative signal
6	BUSB	Analog I/O	-	MIL-STD-1553 bus driver B, positive signal
7	RCVB	Digital output	-	Goes high when MIL-STD-1553 word received on Bus B
8	REG	Digital input	12K pull-down	Selects Status & Mode Register when high, or Data registers when low
9	R/$\overline{\text{W}}$	Digital input	12K pull-up	Controls data and sync direction during read or write operations
10	$\overline{\text{STRB}}$	Digital input	12K pull-up	Strobe. Timing input to control register read and write operations
11	MR	Digital input	12K pull-down	Pulse high to reset the HI-1575
12	SYNC	Digital I/O	12K pull-down	Selects transmit sync type on write, indicates received sync type on read.
13-20, 22-29	D15:D0	Digital I/O	12K pull-down	Data bus. D15 (MSB) corresponds to MIL-STD-1553 bit 4
21	GND	Power supply	-	Ground
30	CLK	Digital input	-	12 MHz clock
31	$\overline{\text{CHA}}$/CHB	Digital Input	12K pull-down	Selects MIL-STD-1553 Bus A or Bus B
32	ERROR	Digital output	-	Goes high when a received MIL-STD-1553 word has an encoding error

FUNCTIONAL DESCRIPTION

Figure 1 shows a simplified block diagram of the HI-1575.

The MR (Master Reset) input should be pulsed high to initialize the Manchester II Encoder and Decoders. MR also clears the Receive Data registers, RXA and RXB, and sets the Status & Mode register to its default state as described in figure 2.

The CLK input requires a 12.0 MHz clock signal. CLK is used to derive the 1.0 us bit period for MIL-STD-1553 data transmission, as well to provide the master clock for the Manchester II encoder and the decoder's receiver sampling logic.

STATUS & MODE REGISTER

The HI-1575 is configured by writing bits 0 - 5 of the Status & Mode (SAM) register. Refer to figure 2 for a complete description. SAM bits 0 - 5 are read/write allowing the user to verify the chip's configuration at any time by reading the SAM. SAM is accessed by performing a read or write cycle with the REG input high.

SAM bits 6 - 15 are read-only and are used to provide status information.

To minimize the number of hardware control inputs, SAM bit 5 (Channel A/B select) is logically 'OR'ed with the $\overline{\text{CHA}}$/CHB input pin. To select between MIL-STD-1553 bus A or B, the user may either tie the $\overline{\text{CHA}}$/CHB pin low and select buses using SAM bit 5 (software control), or program SAM bit 5 to a zero and use the $\overline{\text{CHA}}$/CHB pin to select the active bus (hardware control).

Similarly, the SYNC I/O pin may be left open-circuit allowing the transmitter sync to be programmed into SAM bit 4, or SAM bit 4 can be set to zero and the SYNC pin used to set the transmitted SYNC type. Note that SYNC is an I/O pin. It is an input when writing data to the HI-1575 transmit data register (TX), and an output when reading data from the HI-1575 receivers (RXA and RXB). The SYNC pin must not be shorted directly to VDD or GND. An internal pull-down resistor allow the SYNC pin to be left open-circuit if the user opts for purely software control.

TRANSMITTER

Data words to be transmitted on the MIL-STD-1553 data bus are written to the TX register by pulsing $\overline{\text{STRB}}$ low while R/$\overline{\text{W}}$ is low and REG is low. The logical OR of the $\overline{\text{CHA}}$/CHB input pin and SAM bit 5 (CHAN) during the write cycle determines whether the word is output on MIL-STD-1553 bus A or B. Setting $\overline{\text{CHA}}$/CHB OR CHAN to a zero selects bus A, and a one selects bus B. The logical OR of the SYNC pin and SAM bit 4 (TXSYNC) during the write cycle defines whether the transmitted word is a MIL-STD-1553 Command or Data word. Setting SYNC to a one causes a Command (or Status) sync to be generated. Setting SYNC to zero selects a Data sync. Note that the SYNC pin is bidirectional. It should be treated as an extension to the 16-bit bidirectional databus (D15:D0) in terms of I/O switching and timing.

The HI-1575 automatically calculates and appends the correct parity bit to the transmitted word. Each word is assigned odd parity as required by MIL-STD-1553.

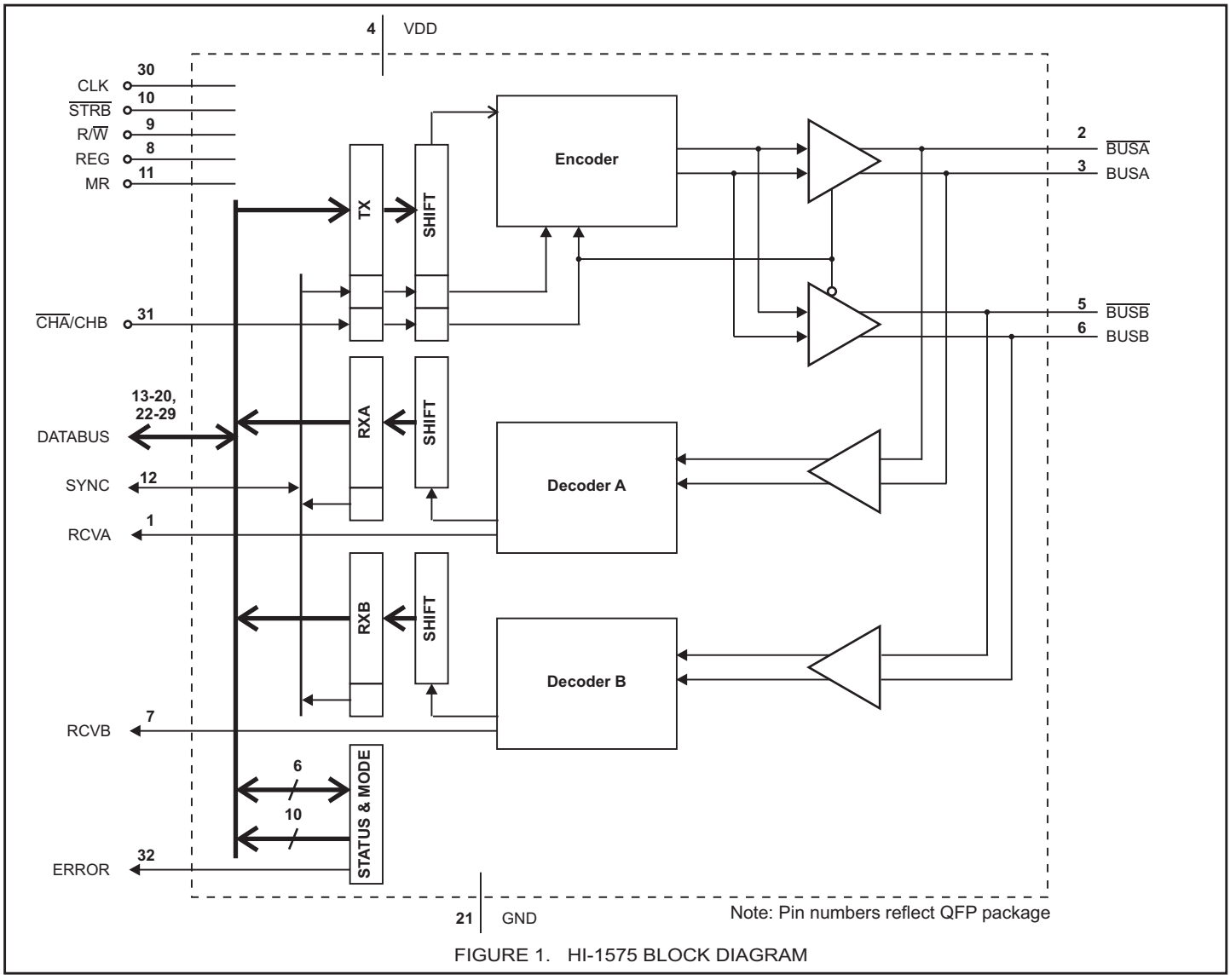


FIGURE 1. HI-1575 BLOCK DIAGRAM

To transmit contiguous words, a second write to the TX register must occur no earlier than 3.5 us and no later than 18.5 us after the first TX write. SAM bit 15 (SENDDATA) is high during this period and may be used as a flag to indicate when the HI-1575 is ready to accept the next data write for contiguous transmission. When transmitting a message of three or more words, the third and subsequent write operations should occur every 20.0 us so as to avoid over-writing the previous data before it is transferred to the transmitter's shift register.

Figure 3 shows a timing diagram for transmit operations.

The transmitter outputs are either direct or transformer coupled to the MIL-STD-1553 data bus. Both coupling methods produce a nominal voltage on the main MIL-STD-1553 bus of 7.5 volts peak-to-peak, line-to-line. Figure 6 shows bus coupling examples.

One or both transmitters may be disabled by writing a '1' into SAM register bits 0 or 1 (TXDISA, TXDISB). When disabled, the host interface works as normal, but there is no output from the BUSA and $\overline{\text{BUSA}}$ (BUSB and $\overline{\text{BUSB}}$) pins.

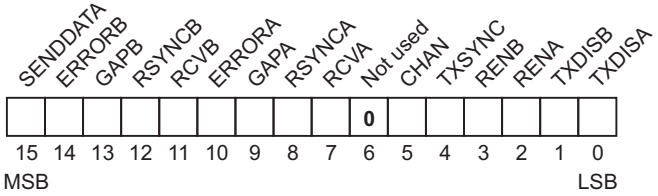
RECEIVER

The HI-1575's two receivers continuously monitor both MIL-STD-1553 data busses. Bi-phase differential data words are accepted from the MIL-STD-1553 bus through the same direct or transformer coupled interface as the transmitter. Each receiver's differential input stage drives a filter and threshold comparator that presents data to the decoders.

The decoder logic checks the incoming word for correct encoding, bit count and parity. If a valid MIL-STD-1553 word is received, the RCVA or RCVB output goes high and the 16-bit received word is transferred to the RXA or RXB register. The HI-1575 ERROR output goes high whenever an encoding error is detected on either bus. If a received word has an encoding error, then SAM bits 10 or 14 (ERRORA, ERRORB) are set high, and the corresponding RCVA or RCVB pin is not asserted.

To minimize the number of pins necessary to interface the HI-1575, the state of RCVA and RCVB can also be read from SAM bits 7 and 11.

STATUS & MODE REGISTER (SAM)



Bit	Name	R/W	Default	Description
0	TXDISA	R/W	0	Writing TXDISA to a '1' disables the transmitter for MIL-STD-1553 bus A
1	TXDISB	R/W	0	Writing TXDISB to a '1' disables the transmitter for MIL-STD-1553 bus B
2	RENA	R/W	1	Setting RENA to a '1' enables the receiver for MIL-STD-1553 bus A. A '0' disables the receiver causing the HI-1575 to ignore all activity on bus A.
3	RENB	R/W	1	Setting RENB to a '1' enables the receiver for MIL-STD-1553 bus B. A '0' disables the receiver causing the HI-1575 to ignore all activity on bus B.
4	TXSYNC	R/W	0	The TXSYNC bit is logically ORed with the SYNC input pin during host write cycles to the Transmit Data Register (TX). If TXSYNC OR SYNC is a '1' the transmitter prefixes the transmitted word with a MIL-STD-1553 Command Sync. If TXSYNC OR SYNC is a '0' during a write to TX, then the transmitted word has a MIL-STD-1553 Data Sync.
5	CHAN	R/W	0	The CHAN bit is logically ORed with the $\overline{\text{CHA}}$/CHB input pin and the result used to Select between MIL-STD-1553 bus A or B during write transfers to the TX register, or reading data from the RX registers. When CHAN OR $\overline{\text{CHA}}$/CHB is a '0' during a transmit operation, data is transmitted on MIL-STD-1553 bus A. When the result is a '1', MIL-STD-1553 bus B is selected. During HI-1575 data read cycles, if CHAN OR $\overline{\text{CHA}}$/CHB is a '0', the RXA register is accessed, and if CHAN OR $\overline{\text{CHA}}$/CHB is a '1' then the data is read from RXB.
6	-	Read-only	0	Not used. Internally set to '0'.
7	RCVA	Read-only	0	This bit reflects the state of the RCVA output pin. RCVA goes high whenever a new word is received on MIL-STD-1553 bus A. The received word may be read by the host from the RXA register. RCVA is reset on reading RXA or if the HI-1575 detects a new word arriving on bus A. If the data words are contiguous, then RCVA will be high for about 3 us before the new word resets it. The data is still available in the RXA register and may be retreived any time up until the RCVA flag goes high again. If the user does not read the data, the word is lost when the RCVA flag goes high on reception of the next word.
8	RSYNCA	Read-only	0	RSYNCA indicates the Sync of the last MIL-STD-1553 word received on bus A. RSYNCA is a '0' for a Data sync, and a '1' for a Command Sync. When the RXA register is read, the RSYNCA value is also output on the SYNC I/O pin.
9	GAPA	Read-only	0	GAPA is a '1' when there is no activity detected on MIL-STD-1553 bus A, for example during an inter-message gap. GAPA is a '0' whenever the HI-1575 detects bus traffic.
10	ERRORA	Read-only	0	ERRORA goes high when the HI-1575 Manchester decoder receives an incorrectly encoded word on MIL-STD-1553 bus A
11	RCVB	Read-only	0	Same function as RCVA but for MIL-STD-1553 bus B.
12	RSYNCB	Read-only	0	Same function as RSYNCA but for MIL-STD-1553 bus B.
13	GAPB	Read-only	0	Same function as GAPA but for MIL-STD-1553 bus B.
14	ERRORB	Read-only	0	Same function as ERRORA but for MIL-STD-1553 bus B.
15	SENDDATA	Read-only	1	SENDDATA goes high approximately 3.5 us after the start of a MIL-STD-1553 word transmission. SENDATA goes low approximately 18.5 us after the start of a MIL-STD-1553 word transmission. If new a new data word is written to the TX register while SENDDATA is high, that word will be transmitted contiguously after the currently transmitting word.

FIGURE 2. STATUS AND MODE REGISTER

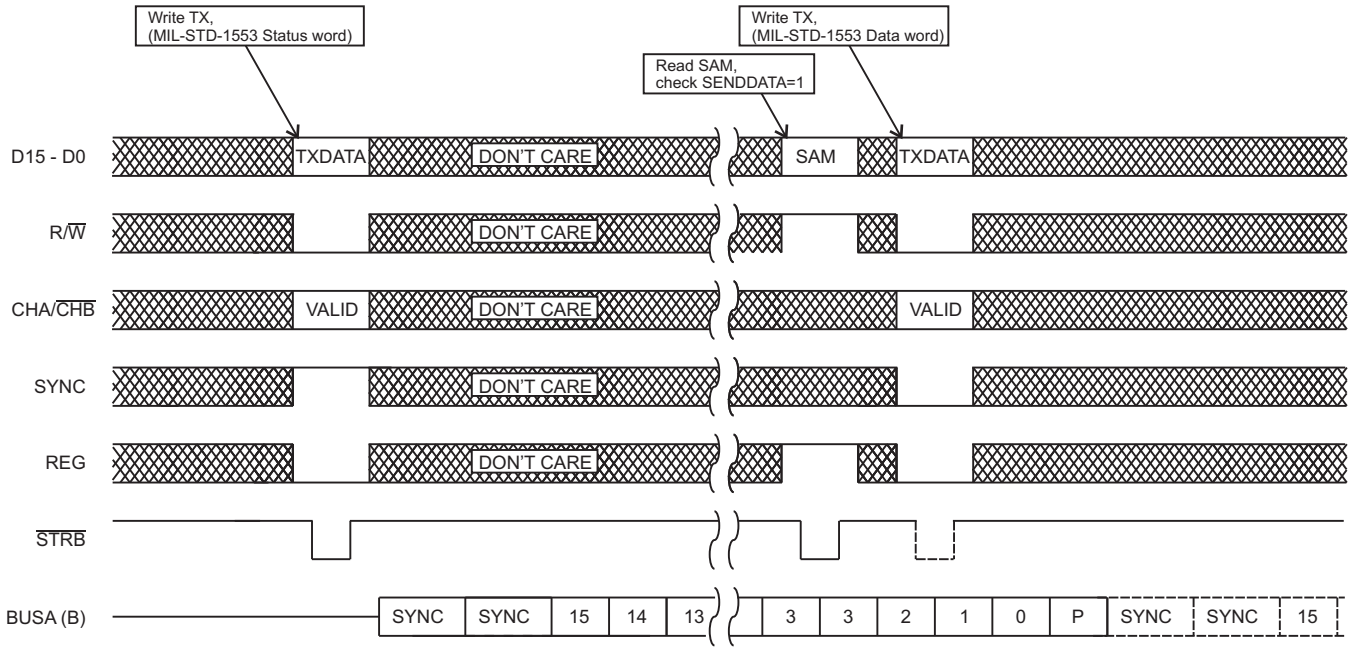


FIGURE 3. EXAMPLE TRANSMIT OPERATION

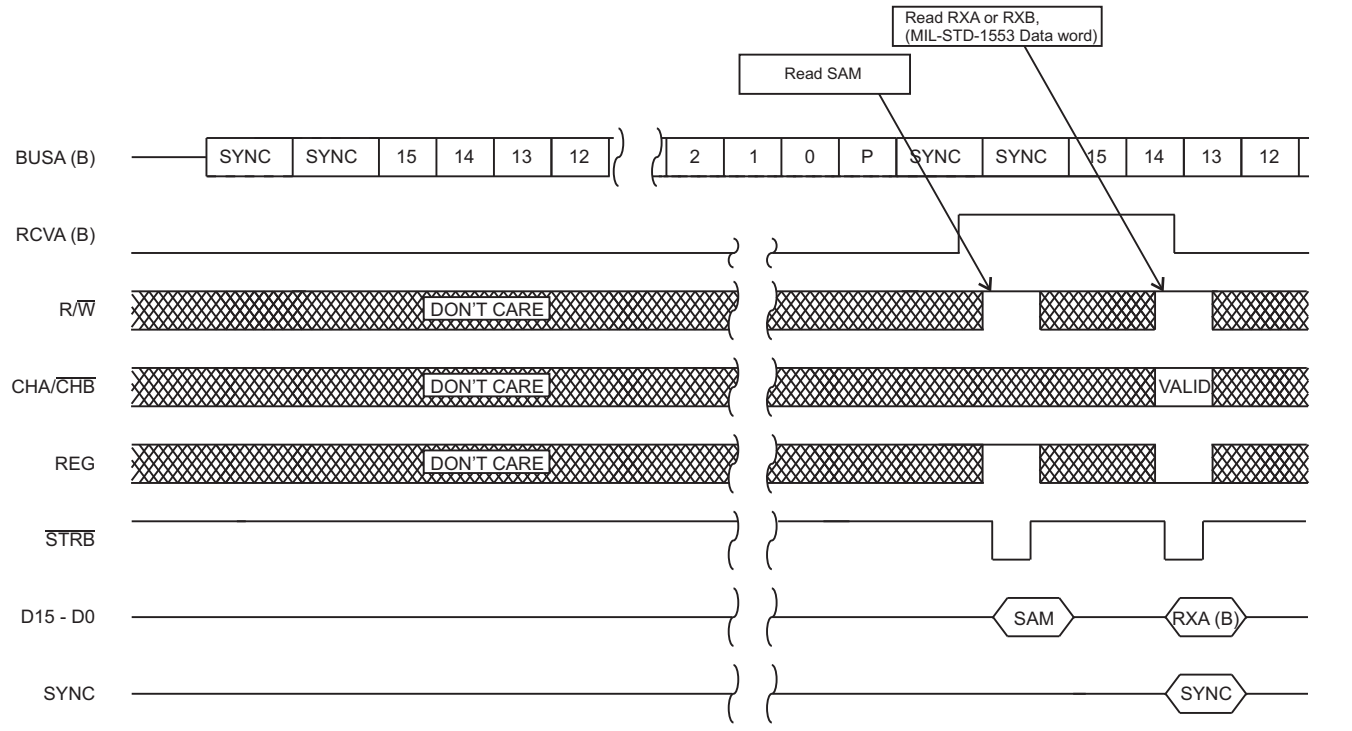


FIGURE 4. EXAMPLE RECEIVE OPERATION

CHAN OR $\overline{CHA}$/CHB	REG	Register
0	0	Receiver A Data (RXA)
1	0	Receiver B Data (RXB)
X	1	Status & Mode Register (SAM)

FIGURE 5. HI-1575 REGISTER MAP

The host reads the received word from the HI-1575 RXA or RXB register. The data word is read by pulsing $\overline{STRB}$ low, while R/$\overline{W}$ is high and REG is low. Figure 4 shows an example receive operation. The SYNC output indicates whether the word had a Command Sync (SYNC=1) or Data Sync (SYNC=0). SAM register bits 8 and 12 (RSYNCA and RSYNCB) retain the Sync values for the last word received on each bus.

SAM bits 2 or 3 (RENA, RENB) can be used to independently enable or disable each receiver. Writing a '1' to RENA enables receiver A. A '0' disables the receiver. RENB performs the same function for the MIL-STD-1553 bus B.

Note that because each receiver is internally connected to its transmitter, when a MIL-STD-1553 word is transmitted by the HI-1575 it will also be received on the same channel. This feature allows the terminal to self-monitor data transmitted to the MIL-STD-1553 data bus.

MIL-STD-1553 BUS CONNECTION

The HI-1575 includes on-chip MIL-STD-1553 analog transceivers which are designed to drive the primary winding of a 1:2.5 turns-ratio MIL-STD-1553 isolation transformer. Figure 6 shows how the HI-1575 may be connected to the MIL-STD-1553 data bus as either a direct coupled stub (Bus A example), or a transformer coupled stub (Bus B example). Holt Integrated Circuits offers a wide range of single-core and dual-core coupling transformers suitable for use with the HI-1575.

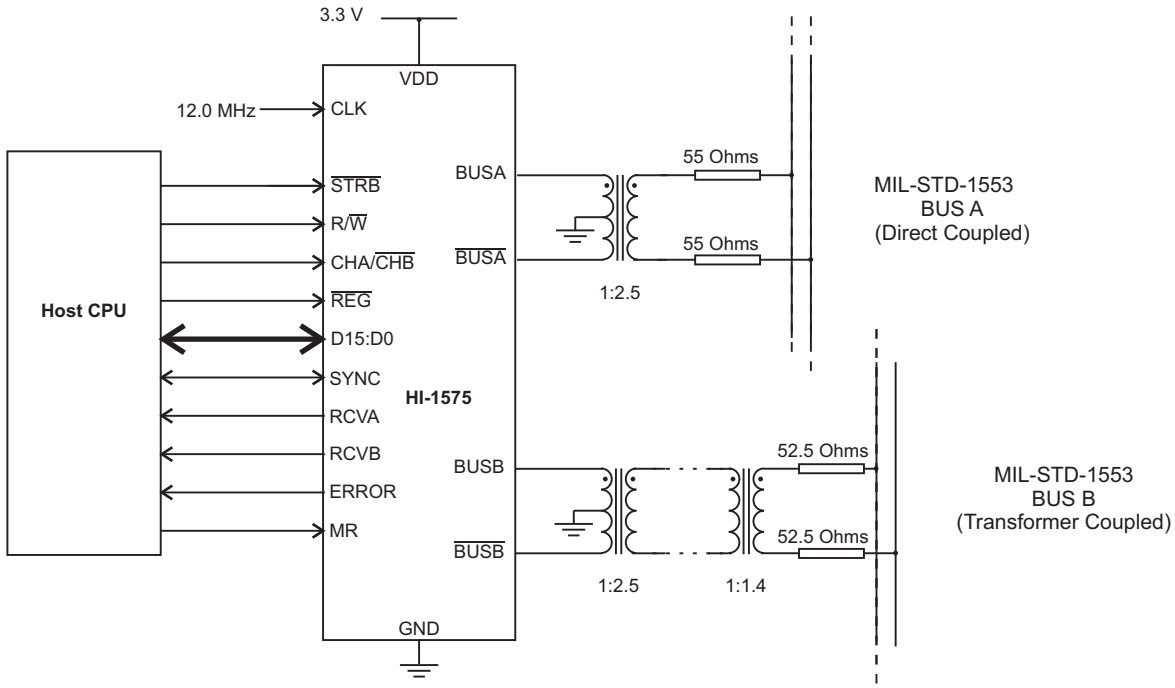


FIGURE 6. MIL-STD-1553 BUS CONNECTION

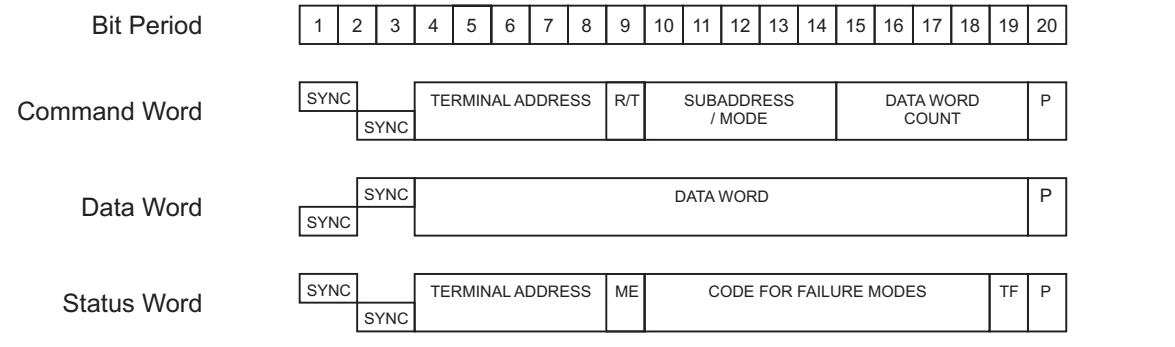


FIGURE 7. MIL-STD-1553 WORD FORMATS

TIMING DIAGRAMS

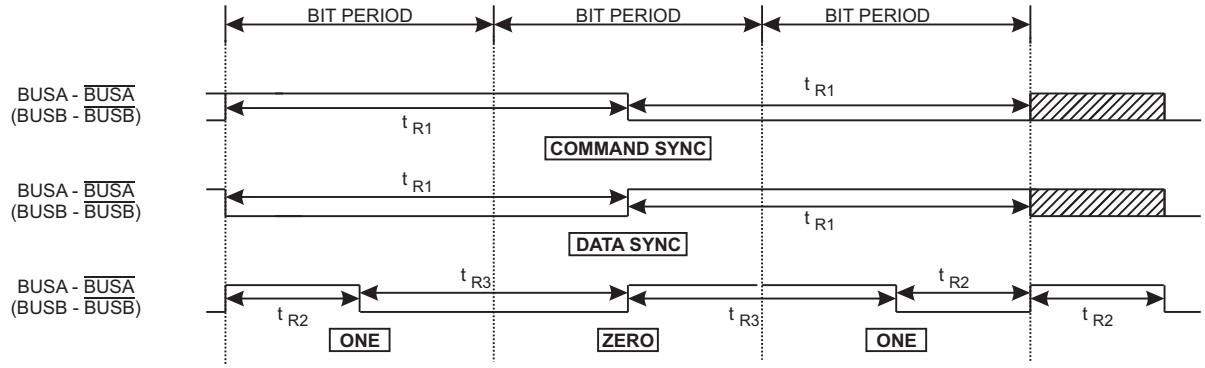


FIGURE 8. MIL-STD-1553 BUS RECEIVER TIMING

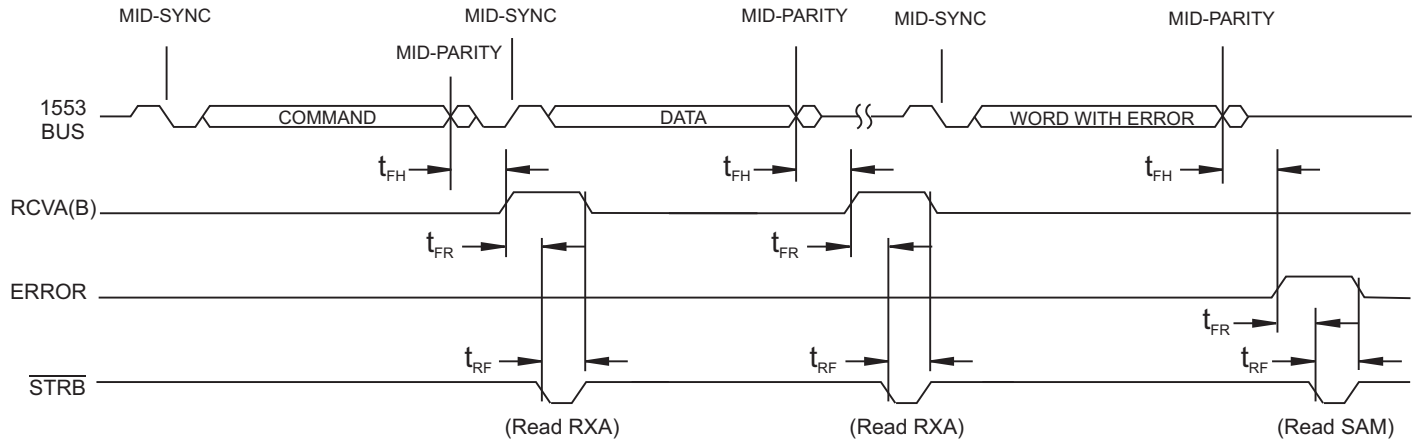


FIGURE 9. HI-1575 RECEIVER TIMING

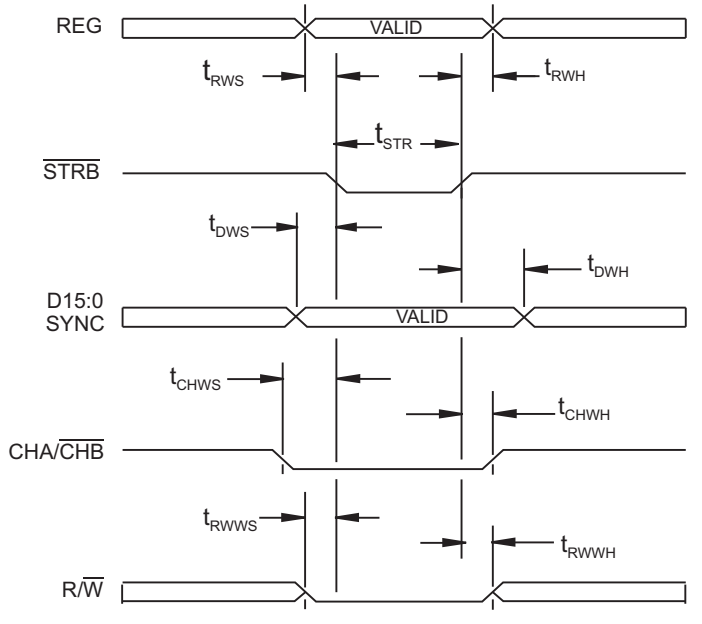


Figure 10. DATABUS TIMING - WRITE.

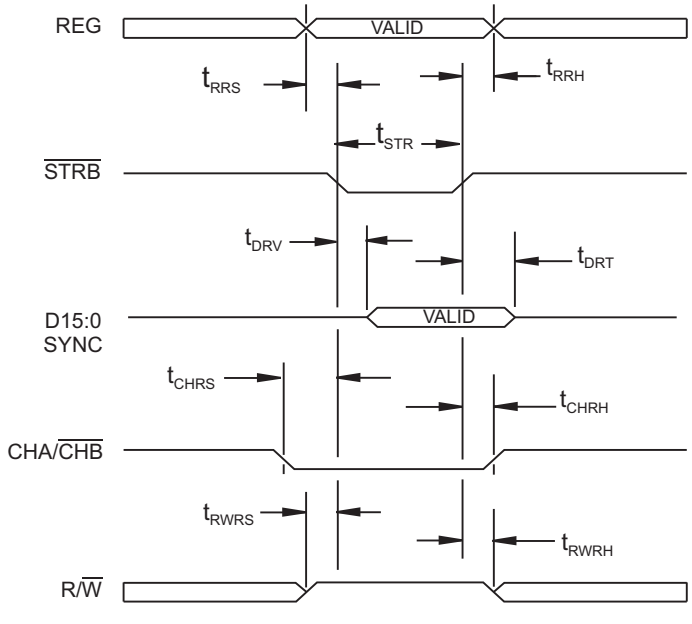


Figure 11. DATABUS TIMING - READ

ABSOLUTE MAXIMUM RATINGS

Supply voltage (VDD)	-0.3 V to +5 V
Logic input voltage range	-0.3 V DC to +3.6 V
Receiver differential voltage	50 Vp-p
Driver peak output current	+1.0 A
Power dissipation at 25°C	1.0 W
Solder Temperature	275°C for 10 sec.
Junction Temperature	175°C
Storage Temperature	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage
VDD..... 3.3V... ±5%

Temperature Range
Industrial Screening.....-40°C to +85°C
Hi-Temp Screening.....-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC ELECTRICAL CHARACTERISTICS

VDD = 3.3 V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Operating Voltage	V_{DD}		3.15	3.30	3.45	V
Total Supply Current	I_{CC1}	Not Transmitting		4	10	mA
	I_{CC2}	Transmit one channel @ 50% duty cycle		225	250	mA
	I_{CC3}	Transmit one channel @ 100% duty cycle		425	500	mA
Power Dissipation	P_{D1}	Not Transmitting			0.06	W
	P_{D2}	Transmit one channel @ 100% duty cycle		0.3	0.5	W
Min. Input Voltage (HI)	V_{IH}	Digital inputs	70%			V_{DD}
Max. Input Voltage (LO)	V_{IL}	Digital inputs			30%	V_{DD}
Min. Input Current (HI)	I_{IH}	Digital inputs (without pull-down)			20	µA
Max. Input Current (LO)	I_{IL}	Digital inputs (without pull-up)	-20			µA
Pull-up / Pull-down current	I_{PUD}	Digital inputs and data bus		275		uA
Min. Output Voltage (HI)	V_{OH}	I_{OUT} = -1.0mA, Digital outputs	90%			V_{DD}
Max. Output Voltage (LO)	V_{IH}	I_{OUT} = 1.0mA, Digital outputs			10%	V_{DD}
RECEIVER (Measured at Point "A_D" in Figure 12 unless otherwise specified)						
Input resistance	R_{IN}	Differential	2			Kohm
Input capacitance	C_{IN}	Differential			5	pF
Common mode rejection ratio	C_{MRR}		40			dB
Input common mode voltage	V_{ICM}		-10.0		+10.0	V-pk
Threshold Voltage - Direct-coupled Detect	V_{THD}	1 Mhz Sine Wave (Measured at Point "A_D" in Figure 12)	1.15			Vp-p
No Detect	V_{THND}				0.28	Vp-p
Theshold Voltage - Transformer-coupled Detect	V_{THD}	1 MHz Sine Wave (Measured at Point "A_T" in Figure 13)	0.86			Vp-p
No Detect	V_{THND}				0.20	Vp-p
TRANSMITTER(Measured at Point "A_D" in Figure 12 unless otherwise specified)						
Output Voltage Direct coupled	V_{OUT}	35 ohm load (Measured at Point "A_D" in Figure 12)	6.0		9.0	Vp-p
Transformer coupled	V_{OUT}	70 ohm load (Measured at Point "A_T" in Figure 13)	18.0		27.0	Vp-p
Output Noise	V_{ON}	Differential, inhibited			10.0	mVp-p
Output Dynamic Offset Voltage Direct coupled	V_{DYN}	35 ohm load (Measured at Point "A_D" in Figure 12)	-90		90	mV
Transformer coupled	V_{DYN}	70 ohm load (Measured at Point "A_T" in Figure 13)	-250		250	mV

AC ELECTRICAL CHARACTERISTICS

VDD = 3.3 V, GND = 0V, T_A =Operating Temperature Range (unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER (Measured at Point "AD" in Figure 12)						
RiseTtime	tr	35 ohm load	100		300	ns
Fall Time	tf	35 ohm load	100		300	ns
RECEIVER (See figures 8 and 9)						
Sync Transition Span	t_{R1}			1500		ns
Short Data Transition Span	t_{R2}			500		ns
Long Data Transition Span	t_{R3}			1000		ns
Delay Mid-Parity to Flag Set	t_{FH}				2500	ns
Flag Setup Time to Read	t_{FR}		0			ns
Flag Reset Delay	t_{RF}				60	ns
DATA BUS TIMING - WRITE (See figure 10)						
Strobe $\overline{STRB}$ Pulse Width	t_{STR}		50			ns
REG Write Setup Time	t_{RWS}		50			ns
REG Write Hold Time	t_{RWH}		10			ns
Databus / SYNC Write Setup Time	t_{DWS}		50			ns
Databus / SYNC Write Hold Time	t_{DWH}		10			ns
CHA/$\overline{CHB}$ Write Setup Time	t_{CHWS}		50			ns
CHA/$\overline{CHB}$ Write Hold Time	t_{CHWH}		10			ns
R/$\overline{W}$ Write Setup Time	t_{RWWS}		50			ns
R/$\overline{W}$ Write Hold Time	t_{RWWH}		10			ns
DATA BUS TIMING - READ (See figure 11)						
Strobe $\overline{STRB}$ Pulse Width	t_{STR}		50			ns
REG Read Setup Time	t_{RRS}		50			ns
REG Read Hold Time	t_{RRH}		10			ns
Data Read to Databus Valid	t_{DRV}				60	ns
Data Read to Databus Tri-state	t_{DRT}		0		60	ns
CHA/$\overline{CHB}$ Read Setup Time	t_{CHRS}		50			ns
CHA/$\overline{CHB}$ Read Hold Time	t_{CHRH}		10			ns
R/$\overline{W}$ Read Setup Time	t_{RWRS}		50			ns
R/$\overline{W}$ Read Hold Time	t_{RWRH}		10			ns

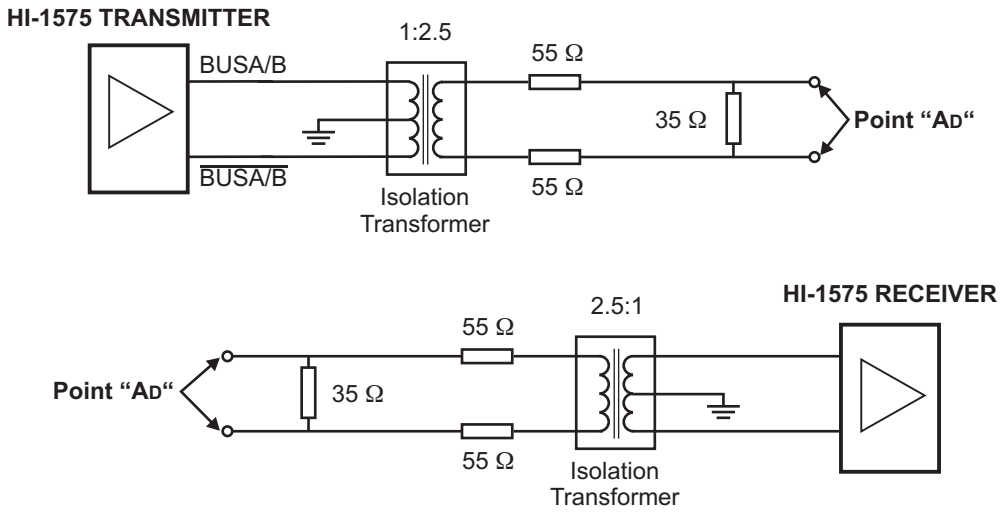


FIGURE 12. DIRECT COUPLED TEST CIRCUITS

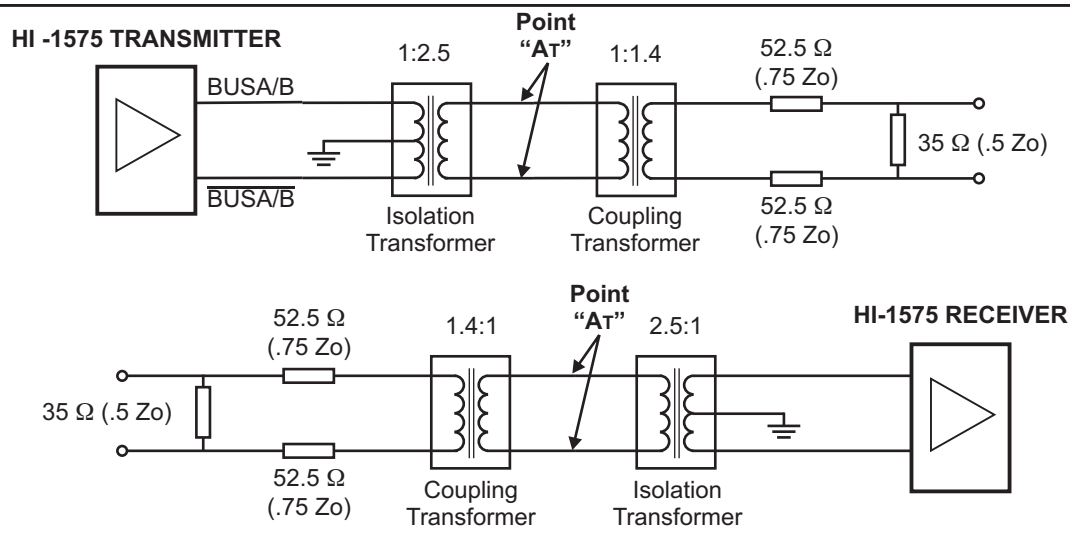


FIGURE 13. TRANSFORMER COUPLED TEST CIRCUITS

HEAT SINKING THE LEADLESS PLASTIC CHIP CARRIER PACKAGE

The HI-1575PCI/T is packaged in a 40 pin leadless plastic chip carrier (QFN). This package has a metal heat sink pad on its bottom surface, which should be soldered to the printed circuit board for optimum thermal dissipation. The package heat sink is electrically isolated and may be soldered to any convenient power plane or ground plane. Redundant "vias" between the exposed board surface and buried power or ground plane will enhance thermal conductivity.

APPLICATIONS NOTE

Holt Applications Note AN-500 provides circuit design notes regarding the use of Holt MIL-STD-1553 data communications devices. Layout considerations, as well as recommended interface and protection components are included.

THERMAL CHARACTERISTICS

PART NUMBER	PACKAGE STYLE	CONDITION	θ_{JA}
HI-1575PQI / T	32 pin PQFP	Mounted on circuit board	59.5 °C / W
HI-1575PCI / T	40 pin LPCC	Heat sink pad soldered	27.5 °C / W

ORDERING INFORMATION

HI - 1575 xx x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO
M	-55°C TO +125°C	M	YES

PART NUMBER	PACKAGE DESCRIPTION
PQ	32 PIN PLASTIC PQFP (32PTQS)
PC	40 PIN CHIP SCALE PACKAGE (40PCS) (PCM not available)

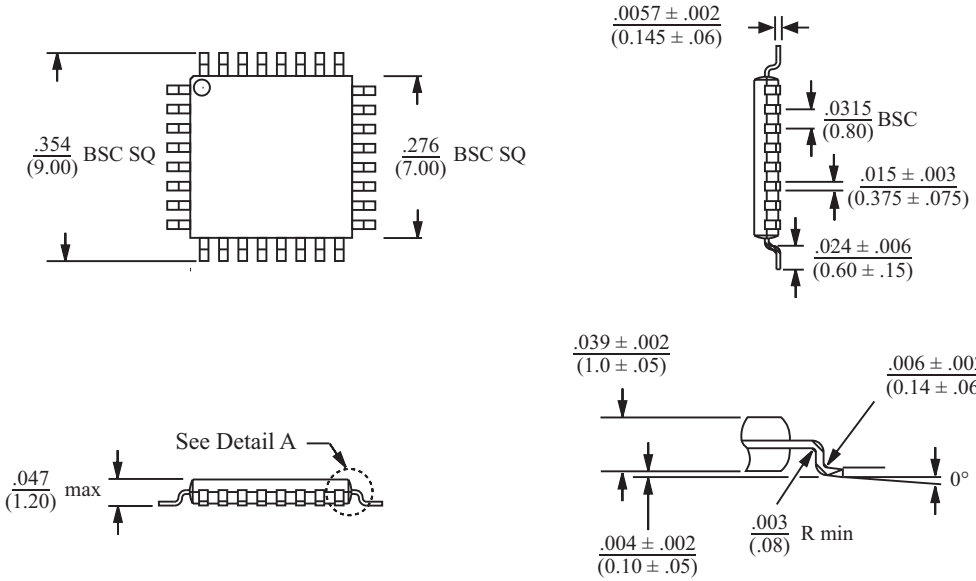
REVISION HISTORY

P/N	Rev	Date	Description of Change
DS1575	D	04/20/11	Added REG input to block diagram. Corrected D.C. Electrical Characteristics Table and package thickness dimension for the 32PTQS.

32 PIN PLASTIC QUAD FLAT PACK (PQFP)

inches (millimeters)

Package Type: 32PQS



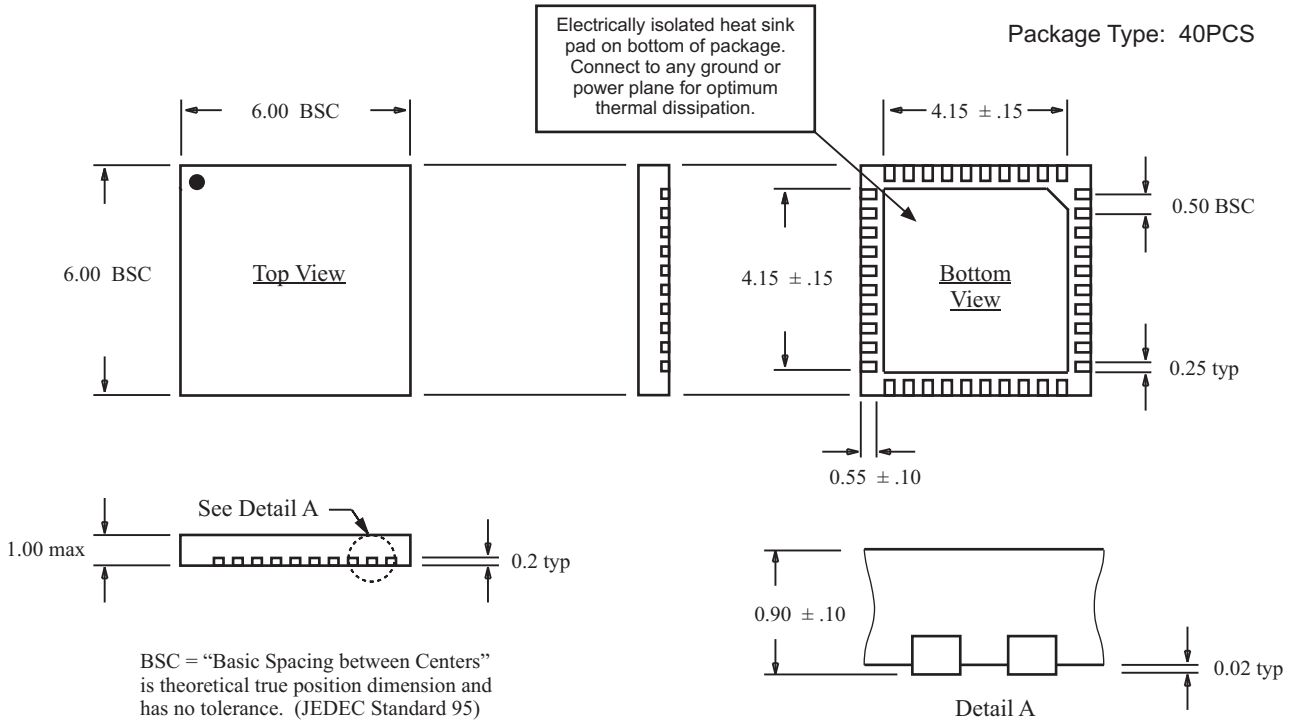
Detail A

BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

40-PIN PLASTIC CHIP-SCALE PACKAGE

millimeters

Package Type: 40PCS



Detail A

BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)