

February 2009

DESCRIPTION

The HI-8787 and HI-8788 are system components for interfacing 16 bit parallel data to an ARINC 429 bus. They combine logic and line driver on one chip. The HI-8787 has an output resistance of 37.5 ohms, and the HI-8788 has an output resistance of 10 ohms to facilitate external lightning protection circuitry. The technology is analog/digital CMOS.

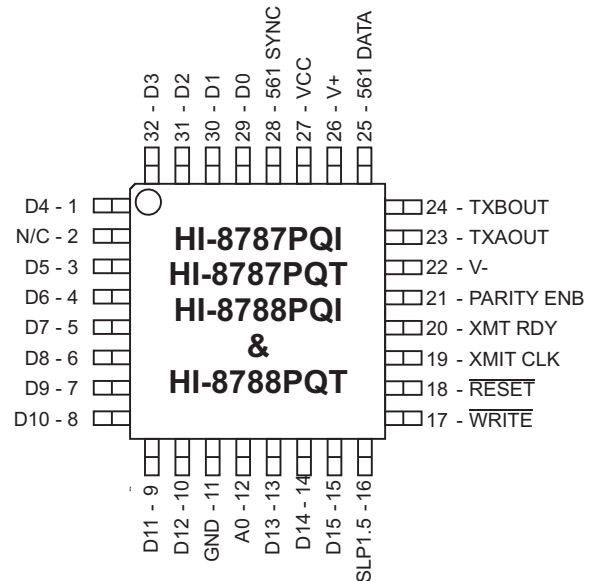
Both products offer high speed data bus transactions into a buffer register. After loading 2 each 16-bit words, data is automatically transferred and transmitted. The data rate is equal to the clock rate. Parity can be enabled in the 32nd bit. Reset is used to initialize the logic upon startup. Word gaps are sent automatically.

The part requires +/- 10 volt supplies in addition to a 5 volt supply.

FEATURES

- Automatically converts 16 bit parallel data to ARINC 429 or 561 serial data
- High speed data bus interface
- On-chip line driver
- Available in small TQFP package
- Industrial and extended temperature ranges

PIN CONFIGURATION



32-Pin Plastic PQFP package

PIN DESCRIPTIONS

| PIN | SYMBOL | FUNCTION | DESCRIPTION |
|----------------------|---------------------------|----------------|---|
| 28 | 561 SYNC | digital output | ARINC 561 Sync signal |
| 1, 3-10,13-15, 29-32 | Dn | digital inputs | Parallel 16 bit bus input |
| 11 | GND | power supply | Ground |
| 12 | A0 | digital input | Load address, A0=1 for 1st data load, A0=0 for 2nd data load |
| 16 | SLP1.5 | digital input | Selects the slope of the line driver. High=1.5us |
| 17 | $\overline{\text{WRITE}}$ | digital input | Write strobe. Loads data on rising edge. |
| 18 | $\overline{\text{RESET}}$ | digital input | Registers and sequencing logic initialized when low |
| 19 | XMIT CLK | digital input | Clock input for the transmitter |
| 20 | XMT RDY | digital output | Goes high if the buffer register is empty |
| 21 | PARITY ENB | digital input | When high the 32nd bit output is odd parity |
| 22 | V- | power supply | -10 volt rail |
| 23 | TXAOUT | analog output | Line driver output - A side |
| 24 | TXBOUT | analog output | Line driver output - B side |
| 25 | 561 DATA | digital output | Serial output for ARINC 561 data |
| 26 | V+ | power supply | +10 volt rail |
| 27 | VCC | power supply | +5 volt rail, "one" level out of line driver, inverted for "zero" |

FUNCTIONAL DESCRIPTION

The HI-8787 is a parallel to serial converter, which when loaded with two 16 bit parallel words, outputs the data as a 32 bit serial word. Timing circuitry inserts a 4 bit gap at the end of each 32 bit word. An input buffer register allows load operations to take place while the previously loaded word is being transmitted.

If the PARITY ENB pin is high, the 32nd bit will be a parity bit, inserted so as to make the 32 bit word have odd parity. If the PARITY ENB pin is low, the 32nd bit will be the D15 bit of the 2nd word loaded.

Outputs are provided for both ARINC 429 (TXAOUT and TXBOUT pins) and ARINC 561 (561 DATA and 561 SYNC pins) type data.

A low signal applied to the $\overline{\text{RESET}}$ pin resets the HI-8787's internal logic so that spurious transmission does not take place during power-up. The registers are cleared so that a continuous gap will be transmitted until the first word is loaded into the transmitter.

The XMIT CLK frequency is the same as the data rate.

Input data can be loaded when the XMT RDY signal is high, which indicates the input buffer register is empty. The first 16 bit word is loaded with the A0 input high. The second word is loaded with A0 in the low state. Once A0 is set low, it must not go high until after the second byte is loaded. Each data word is loaded into the input buffer register by a low pulse on the $\overline{\text{WRITE}}$ input. After the second word has been loaded, the XMT RDY output goes low.

The contents of the input buffer register are transferred to the output register during the fourth bit period of the gap. If the fourth gap bit period of the previous word has already been transmitted, the contents of the input buffer register will be transferred to the output shift register during the first bit period after the second data load, and the XMT RDY output goes high.

After the output shift register is loaded, the data is shifted out to the output logic in the order shown in figure 2.

The 561 SYNC output pulses low when the XMIT CLK is low during the 8th bit of the ARINC transmission.

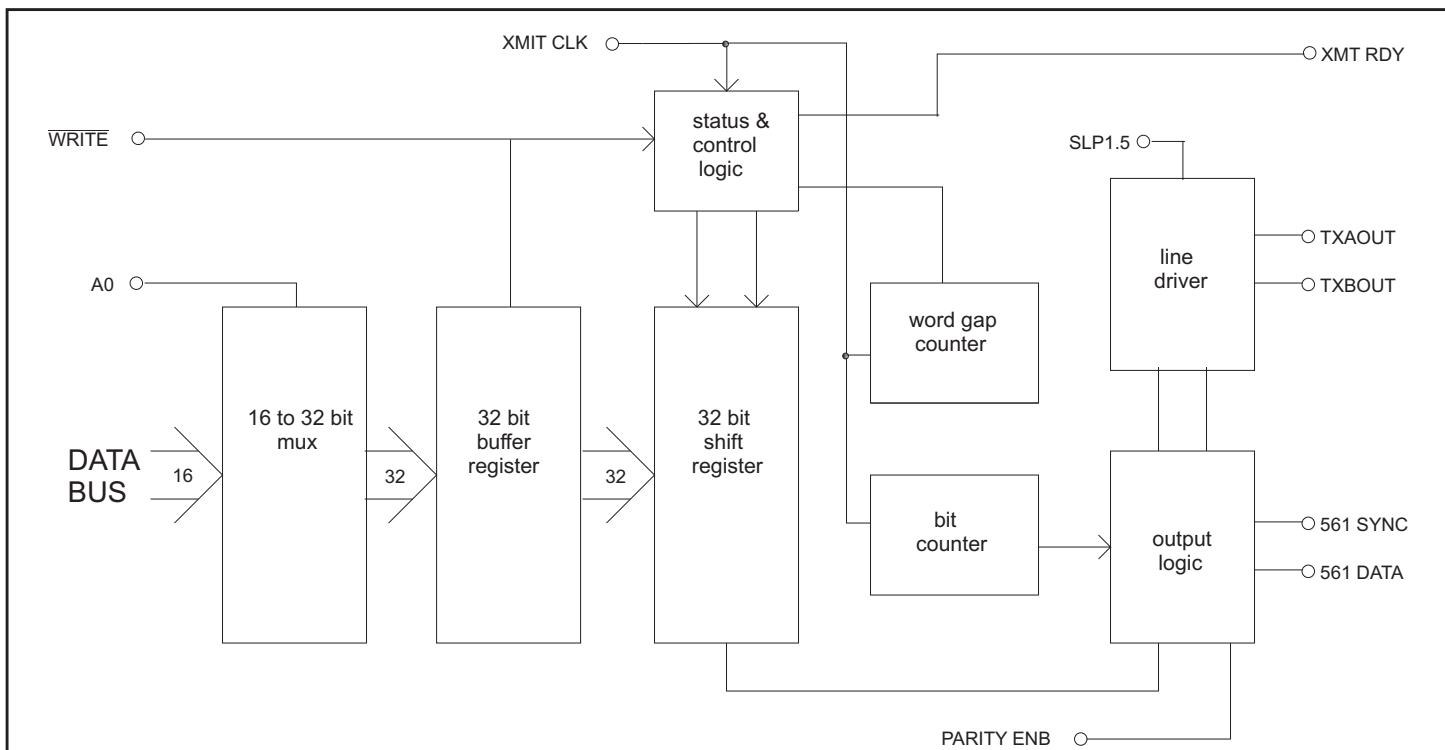


Figure 1. Block Diagram

FUNCTIONAL DESCRIPTION (Cont.)

The HI-8787 and HI-8788 have an on-chip line driver designed to directly drive the ARINC 429 bus. The two ARINC outputs (TXAOUT and TXBOUT) provide a differential voltage to produce a +10 volt One, a -10 volt Zero, and a 0 volt Null. The slope of the ARINC outputs is controlled by the SLP1.5 pin. If SLP1.5 is high, the output rise and fall time is nominally 1.5µs. If SLP1.5 is set low, the rise and fall times are 10µs.

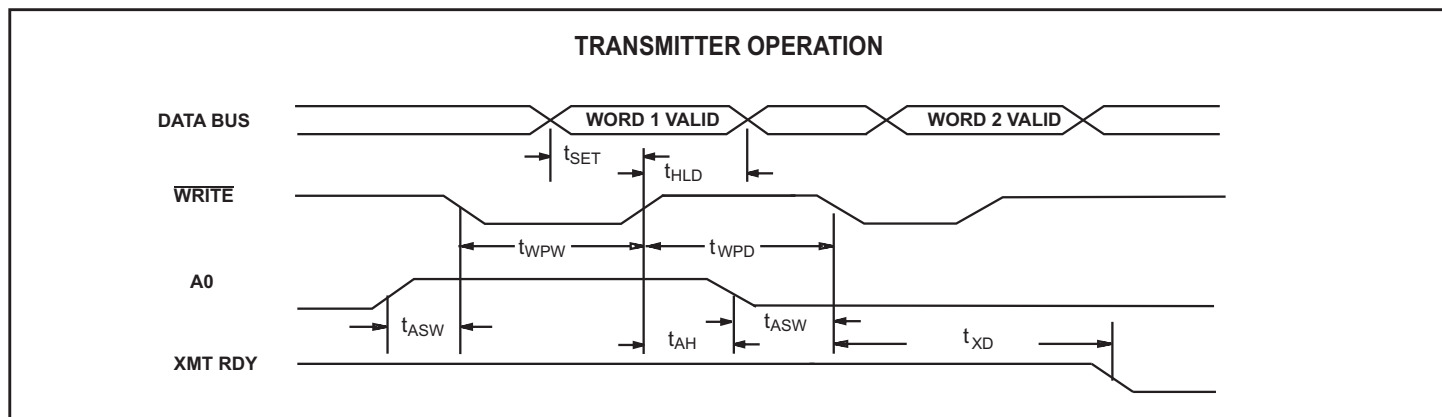
The HI-8787 has 37.5 ohms in series with each line driver output. The HI-8788 has 10.0 ohms in series. The HI-8788 is for applications where external series resistance is needed, typically for lightning protection devices.

| A0 | Load | Data Bus | ARINC Bits |
|----|--------|----------|---------------------|
| 1 | Word 1 | D0 - D15 | ARINC 1 - ARINC 16 |
| 0 | Word 2 | D0 - D15 | ARINC 17 - ARINC 32 |

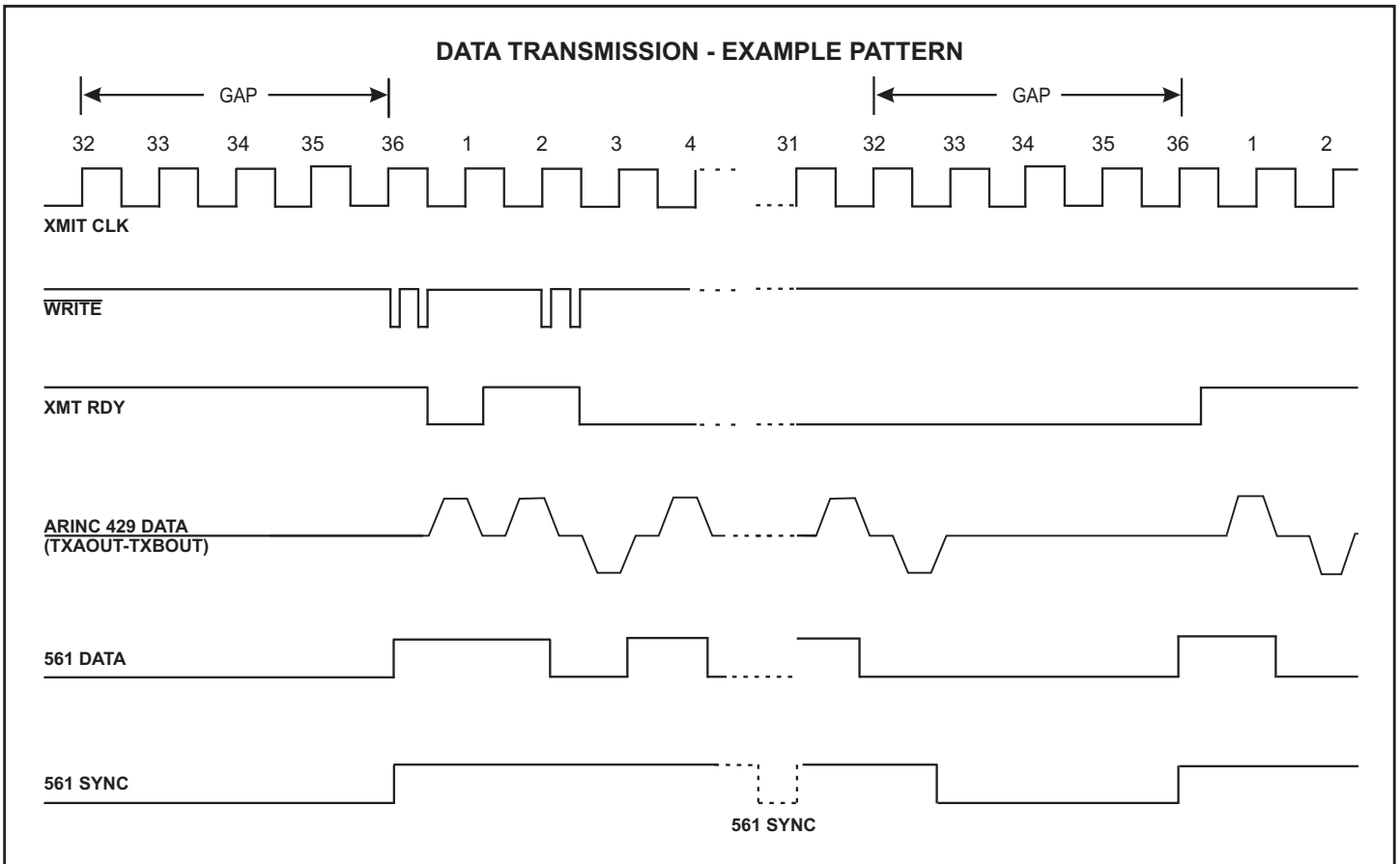
Figure 2. Order of transmitted data

POWER SUPPLY SEQUENCING

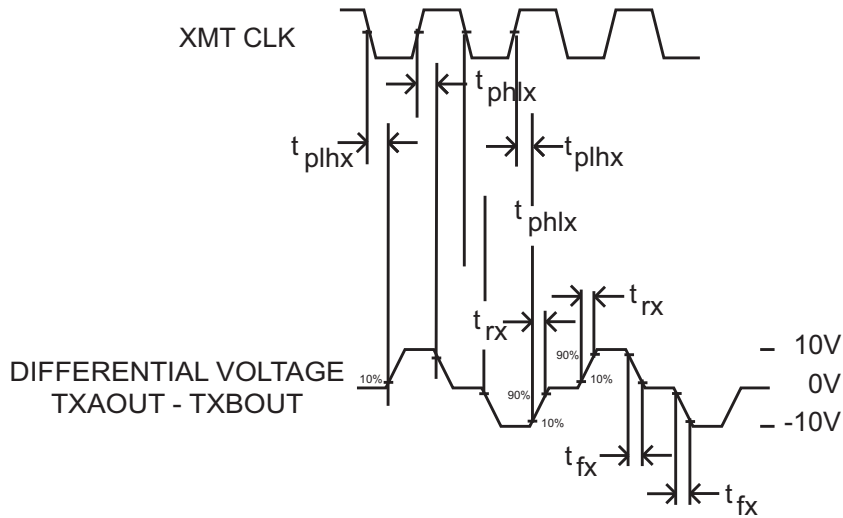
The power supplies must be controlled to prevent large currents during supply turn-on and turn-off. The required sequence is V+ followed by VCC, always ensuring that V+ is the most positive supply. The V- supply is not critical and can be asserted at any time.



DATA TRANSMISSION - EXAMPLE PATTERN



LINE DRIVER OUTPUTS



ABSOLUTE MAXIMUM RATINGS

Voltages referenced to Ground

| | |
|-------------------------------|----------------------|
| Supply voltages | |
| V+..... | 12.5V |
| V-..... | -12.5V |
| VCC..... | 7V |
| DC current per input pin..... | +10ma |
| Power dissipation at 25° | |
| plastic DIL..... | 1.0W, derate 10mW/°C |
| ceramic DIL..... | 0.5W, derate 7mW/°C |
| Solder Temperature | 275°C for 10 sec |
| Storage Temperature..... | -65°C to +150°C |

RECOMMENDED OPERATING CONDITIONS

| | |
|-------------------|-----------------|
| Supply Voltages | |
| V+ | +10V... ±5% |
| V- | -10V... ±5% |
| VCC | 5V... ±5% |
| Temperature Range | |
| Industrial | -40°C to +85°C |
| Extended | -55°C to +125°C |

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC ELECTRICAL CHARACTERISTICS

VCC = 5.0V, Vss = 0V, V+ = 10V, V- = -10V, TA = Operating Temperature Range (unless otherwise specified).

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|--|------------------|---------------------------|-------|-------|------|-------|
| Operating Voltage | Vcc | | 4.75 | 5 | 5.25 | V |
| Operating Voltage | V+ | | 9.5 | 10 | 10.5 | V |
| Operating Voltage | V- | | -9.5 | -10 | 10.5 | V |
| Min. Input Voltage (HI) | V _{IH} | | 2.0 | 1.4 | | V |
| Max. Input Voltage (LO) | V _{IL} | | | 1.4 | 0.7 | V |
| Min. Input Current (HI) | I _{IH} | V _{IH} = 4.9V | | | 280 | µA |
| Max. Input Current (LO) | I _{IL} | V _{IL} = 0.1V | -1 | | | µA |
| Min. Output Voltage (HI) | V _{OH} | I _{OUT} = -1.6mA | 2.7 | | | V |
| Max. Output Voltage (LO) | V _{IH} | I _{OUT} = 1.6mA | | | 0.4 | V |
| Line Driver Output Levels (Ref. To GND) | | | | | | |
| ONE | | no load, VCC = 5.0V | 4.5 | 5.0 | 5.5 | V |
| NULL | | " | -0.25 | 0 | 0.25 | V |
| ZERO | | " | -5.5 | -5.0 | -4.5 | V |
| Line Driver Output Levels (Differential TXAOUT - TXBOUT) | | | | | | |
| ONE | | no load, VCC = 5.0V | 9.0 | 10.0 | 11.0 | V |
| NULL | | " | -0.5 | 0 | 0.5 | V |
| ZERO | | " | -11.0 | -10.0 | -9.0 | V |
| Minimum Short Circuit Sink or Source Current | I _{OUT} | momentary magnitude | 80 | | | mA |
| Operating Current Drain | I _{CC} | f = 100khz | | 0.8 | 2.8 | mA |
| Operating Current Drain (V+) | I _{DD} | f = 100khz | | 6 | 20 | mA |
| Operating Current Drain (V-) | I _{EE} | f = 100khz | -20 | -6 | | mA |
| Input Capacitance | C _{IN} | Not tested | | | 20 | pF |

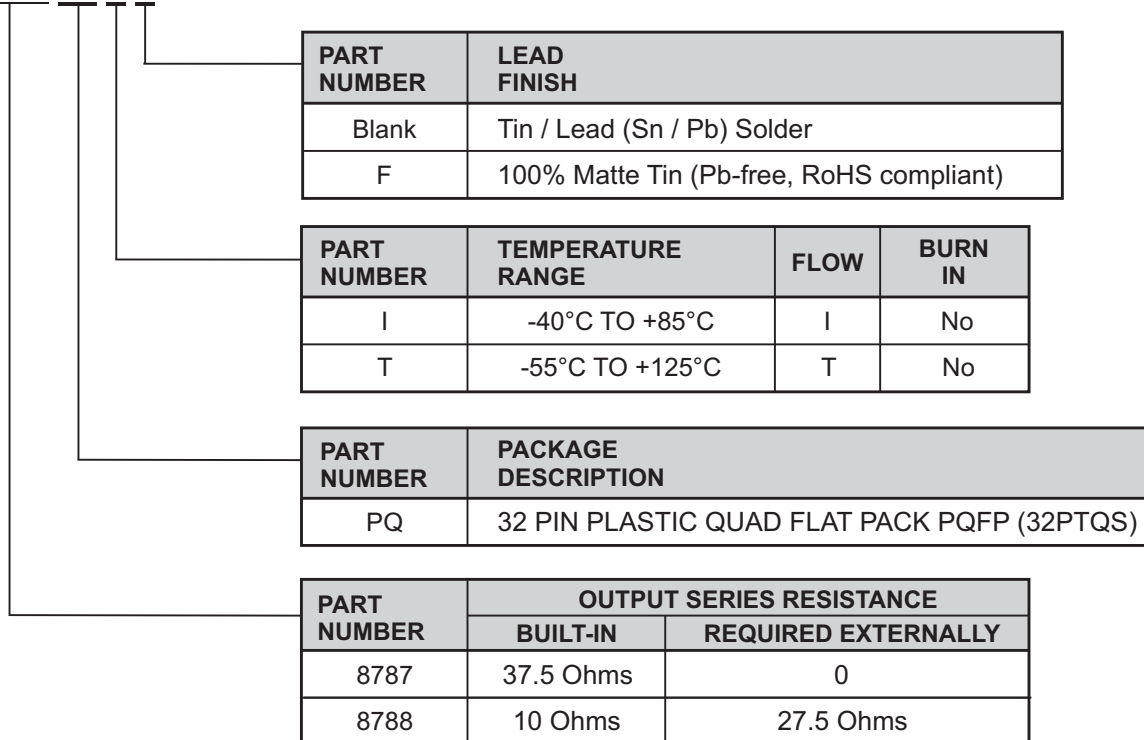
AC ELECTRICAL CHARACTERISTICS

VCC = 5.0V, V+ = 10V, V- = -10V, Vss = 0V, TA = Operating Temperature Range (unless otherwise specified).

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------|------------------|-----|-----|-------|---------------|
| DATA BUS TIMING | | | | | | |
| Setup Data Bus to $\overline{\text{WRITE}}$ | tSET | | 20 | | | ns |
| Hold $\overline{\text{WRITE}}$ to Data Bus | tHLD | | 30 | | | ns |
| Hold A0 to $\overline{\text{WRITE}}$ | tAH | | 0 | | | ns |
| Pulse width $\overline{\text{WRITE}}$ | tWPW | | 40 | | 1 CLK | ns |
| Delay between $\overline{\text{WRITE}}$ | tWPD | | 40 | | | ns |
| Setup A0 to $\overline{\text{WRITE}}$ | tASW | | 20 | | | ns |
| Delay last $\overline{\text{WRITE}}$ to XMT RDY | tXD | | 80 | | | ns |
| LINE DRIVER TIMING | | | | | | |
| Line Driver propagation delay | | No load | | | | |
| Output high to low | tphx | | - | 500 | - | ns |
| Output low to high | tplhx | | - | 500 | - | ns |
| Line Driver transition times | | | | | | |
| Output high to low | t fx | SLP1.5 = logic 1 | 1.0 | 1.5 | 2.0 | μs |
| Output low to high | t rx | SLP1.5 = logic 1 | 1.0 | 1.5 | 2.0 | μs |
| Output high to low | t fx | SLP1.5 = logic 0 | 5 | 10 | 15 | μs |
| Output low to high | t rx | SLP1.5 = logic 0 | 5 | 10 | 15 | μs |

ORDERING INFORMATION

HI - 87xx xx x x



| PART NUMBER | LEAD FINISH |
|-------------|--|
| Blank | Tin / Lead (Sn / Pb) Solder |
| F | 100% Matte Tin (Pb-free, RoHS compliant) |

| PART NUMBER | TEMPERATURE RANGE | FLOW | BURN IN |
|-------------|-------------------|------|---------|
| I | -40°C TO +85°C | I | No |
| T | -55°C TO +125°C | T | No |

| PART NUMBER | PACKAGE DESCRIPTION |
|-------------|---|
| PQ | 32 PIN PLASTIC QUAD FLAT PACK PQFP (32PTQS) |

| PART NUMBER | OUTPUT SERIES RESISTANCE | |
|-------------|--------------------------|---------------------|
| | BUILT-IN | REQUIRED EXTERNALLY |
| 8787 | 37.5 Ohms | 0 |
| 8788 | 10 Ohms | 27.5 Ohms |

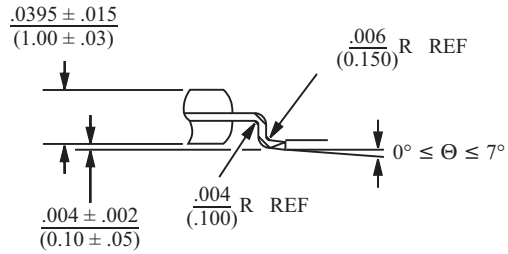
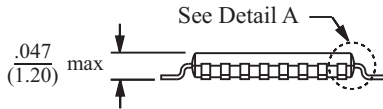
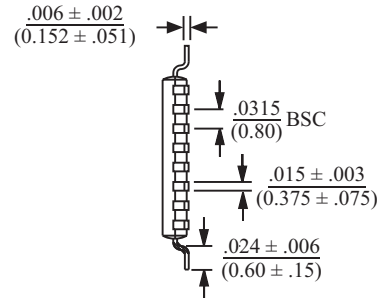
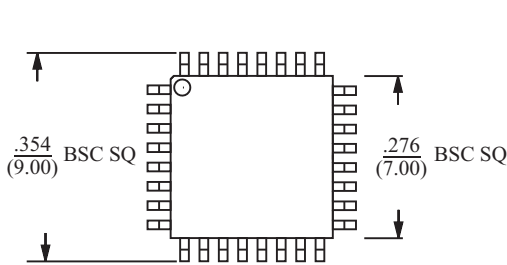
REVISION HISTORY

| Revision | Date | Description of Change |
|----------------|----------|---|
| DS8787, Rev. J | 02/04/09 | Clarified the extended temperature ranges and the power supply nomenclatures in the power sequencing description. |

32 PIN PLASTIC QUAD FLAT PACK (PQFP)

inches (millimeters)

Package Type: 32PTQS



Detail A

BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)