HOLT INTEGRATED CIRCUITS INC.

HI-8470

16-Channel Discrete-to-Digital Sensor with ARINC 429 Transmitter

January 2015

DESCRIPTION

The HI-8470 is a sixteen channel discrete-to-digital interface device. The IC has 16 channels which can sense Open/Ground or 28V/Open signal levels. The voltage threshold of the sensors is user programmable with external resistors. Sense input thresholds may also be set to CMOS logic levels to interface the part with other sensors, for example an external ADC or resolver.

An on-chip ARINC 429 transmitter / line driver allows the status of discrete lines to be transmitted in ARINC 429 format with pin-programmed label byte value, repetition rate and transmission speed. Complete operation of the HI-8470 is controlled by CMOS logic pins, negating the need for a MCU or software in the application.

A single 1 MHz clock source is required for ARINC 429 bit timing and word transmission rate scheduling.

The on-chip ARINC 429 Line Driver operates from a single 3.3V power supply, using an integrated DC/DC converter to generate the required bipolar line voltages.

The discrete sense pins and line driver outputs are lightning protected to RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B) without the use of any external components.

FEATURES

- Pin programmable - **requires no MCU or software control** (no need for DO-178 certification)
- Robust CMOS Silicon-on-Insulator (SOI) technology
- 16 threshold-selectable discrete input channels
- Programmable Thresholds and Hysteresis
- Sense Detection Range 3V to 22V
- On-chip ARINC 429 Transmitter and Line Driver
- 3.3 V single supply operation
- Pin programmable transmit repetition rate
- Internal lightning protection circuitry for both discrete sense lines and line driver allows compliance with RTCA/DO-160G, Section 22 Level 3 Pin Injection Tests.
- Adjustable sense thresholds
- DO-254 certifiable

TYPICAL APPLICATION

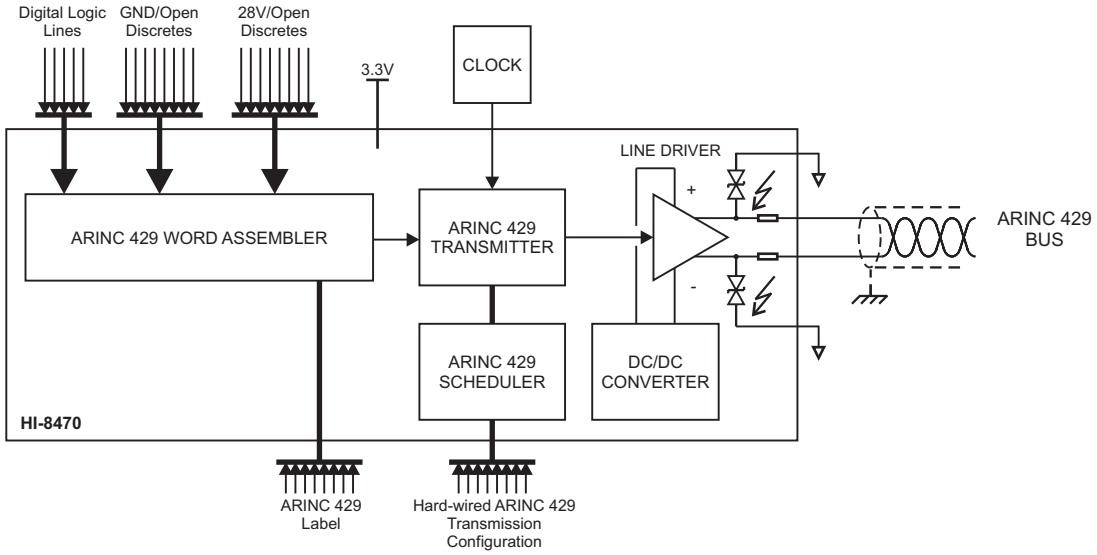


Figure 1

BLOCK DIAGRAM

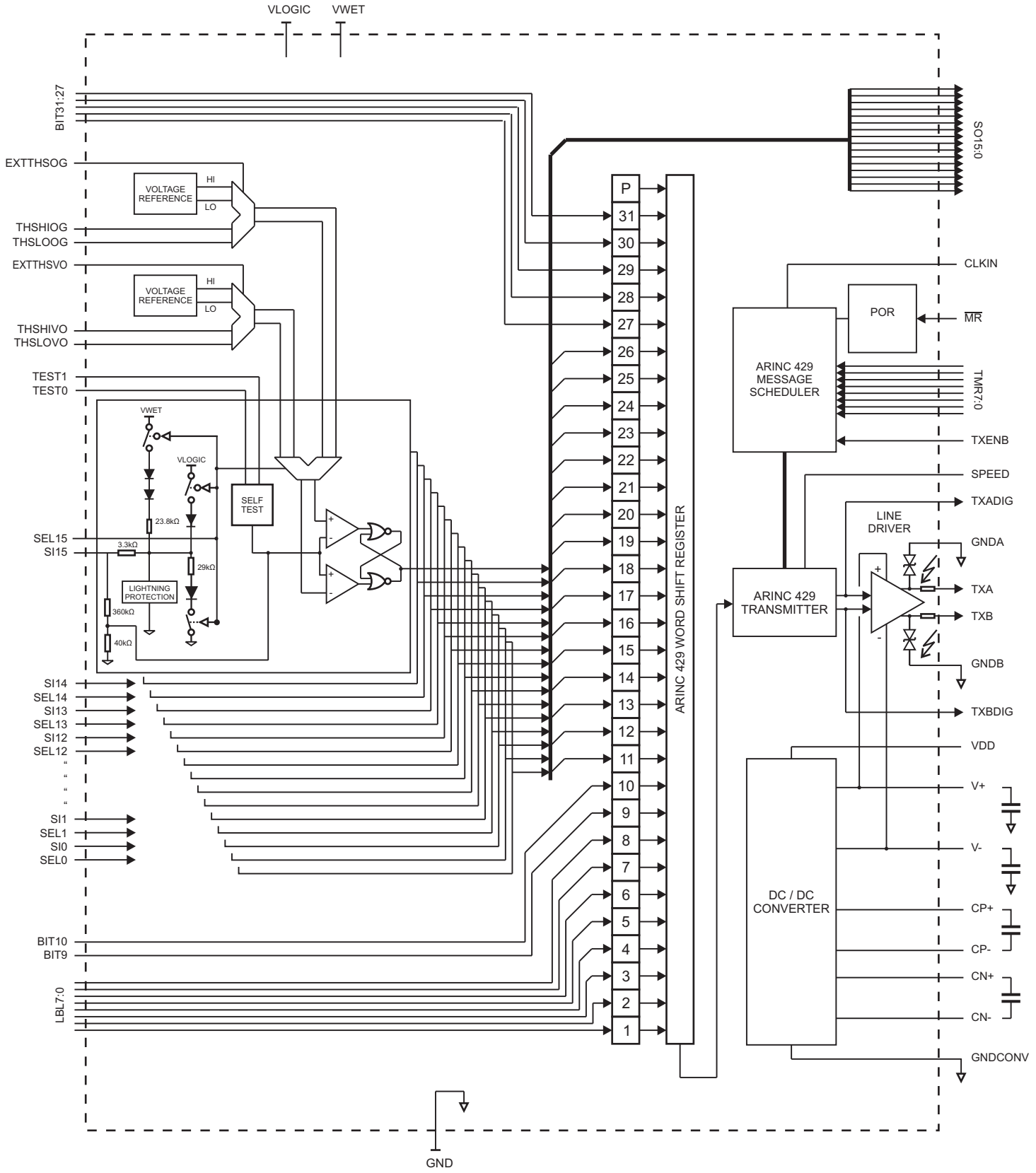


Figure 2

PIN DESCRIPTIONS

PIN	SYMBOL	FUNCTION	DESCRIPTION	PULL UP/DOWN
1	VWET	Supply	Optional input to supply relay wetting current to Sense lines in GND/Open operation	-
2	SI0	Discrete Input	Sense input 0. Mapped SO0 digital output and transmitted ARINC 429 bit 11	None
3	SI1	Discrete Input	Sense input 1. Mapped SO1 digital output and transmitted ARINC 429 bit 12	None
4	SI2	Discrete Input	Sense input 2. Mapped SO2 digital output and transmitted ARINC 429 bit 13	None
5	SI3	Discrete Input	Sense input 3. Mapped SO3 digital output and transmitted ARINC 429 bit 14	None
6	SI4	Discrete Input	Sense input 4. Mapped SO4 digital output and transmitted ARINC 429 bit 15	None
7	SI5	Discrete Input	Sense input 5. Mapped SO5 digital output and transmitted ARINC 429 bit 16	None
8	SI6	Discrete Input	Sense input 6. Mapped SO6 digital output and transmitted ARINC 429 bit 17	None
9	SI7	Discrete Input	Sense input 7. Mapped SO7 digital output and transmitted ARINC 429 bit 18	None
10	SI8	Discrete Input	Sense input 8. Mapped SO8 digital output and transmitted ARINC 429 bit 19	None
11	SI9	Discrete Input	Sense input 9. Mapped SO9 digital output and transmitted ARINC 429 bit 20	None
12	SI10	Discrete Input	Sense input 10. Mapped SO10 digital output and transmitted ARINC 429 bit 21	None
13	SI11	Discrete Input	Sense input 11. Mapped SO11 digital output and transmitted ARINC 429 bit 22	None
14	SI12	Discrete Input	Sense input 12. Mapped SO12 digital output and transmitted ARINC 429 bit 23	None
15	SI13	Discrete Input	Sense input 13. Mapped SO13 digital output and transmitted ARINC 429 bit 24	None
16	SI14	Discrete Input	Sense input 14. Mapped SO14 digital output and transmitted ARINC 429 bit 25	None
17	SI15	Discrete Input	Sense input 15. Mapped SO15 digital output and transmitted ARINC 429 bit 26	None
18	GND	Supply	Logic ground	-
19	TEST0	Digital Input	When high, forces all comparator inputs to ground	30k pull-down
20	TEST1	Digital Input	When high, forces all comparator inputs high	30k pull-down
21	SO0	Digital Output	Sense channel 0 output state	-
22	SO1	Digital Output	Sense channel 1 output state	-
23	SO2	Digital Output	Sense channel 2 output state	-
24	SO3	Digital Output	Sense channel 3 output state	-
25	SO4	Digital Output	Sense channel 4 output state	-
26	SO5	Digital Output	Sense channel 5 output state	-
27	SO6	Digital Output	Sense channel 6 output state	-
28	SO7	Digital Output	Sense channel 7 output state	-
29	SO8	Digital Output	Sense channel 8 output state	-
30	SO9	Digital Output	Sense channel 9 output state	-
31	SO10	Digital Output	Sense channel 10 output state	-
32	SO11	Digital Output	Sense channel 11 output state	-
33	SO12	Digital Output	Sense channel 12 output state	-
34	SO13	Digital Output	Sense channel 13 output state	-
35	SO14	Digital Output	Sense channel 14 output state	-
36	SO15	Digital Output	Sense channel 15 output state	-
37	SPEED	Digital Input	If high ARINC 429 transmission is 100 kbit/s, else 12.5 kbit/s	None
38	$\overline{MR}$	Digital input	Master Reset clears and initializes the transmitter. Active low.	30k pull-up
39	CLKIN	Digital Input	1 MHZ (+/- 1%) must be provided to operate the ARINC429 transmitter	None
40	LBL0	Digital Input	Data for 8th transmitted bit of ARINC 429 word. (Label byte LSB)	None
41	LBL1	Digital input	Data for 7th transmitted bit of ARINC 429 word	None
42	LBL2	Digital input	Data for 6th transmitted bit of ARINC 429 word	None
43	LBL3	Digital input	Data for 5th transmitted bit of ARINC 429 word	None
44	LBL4	Digital input	Data for 4th transmitted bit of ARINC 429 word	None
45	LBL5	Digital input	Data for 3rd transmitted bit of ARINC 429 word	None
46	LBL6	Digital input	Data for 2nd transmitted bit of ARINC 429 word	None
47	LBL7	Digital input	Data for 1st transmitted bit of ARINC 429 word. (Label byte MSB)	None

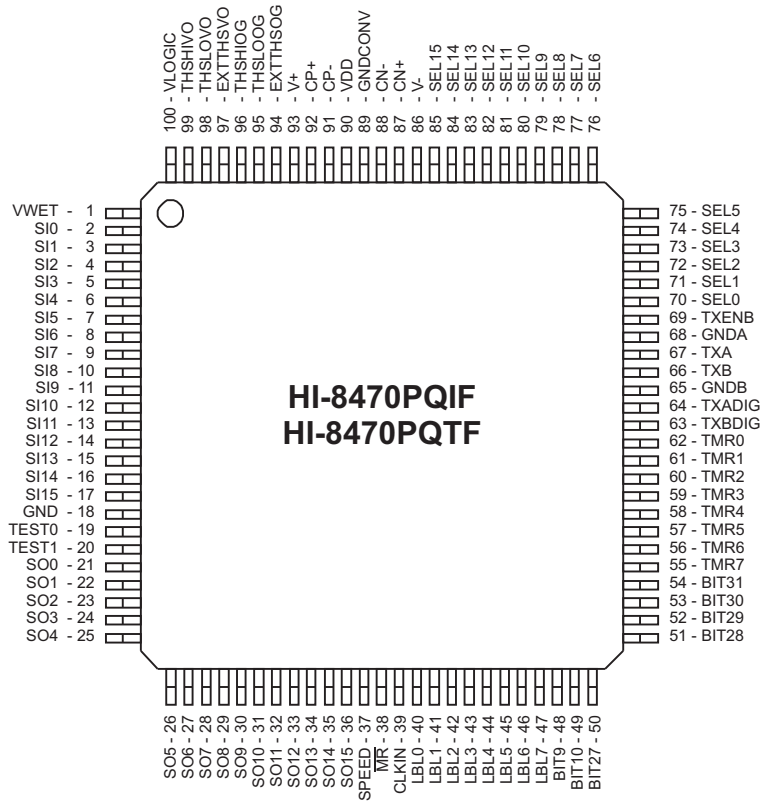
PIN DESCRIPTIONS

PIN	SYMBOL	FUNCTION	DESCRIPTION	PULL UP/DOWN
48	BIT9	Digital Input	Data for 9th transmitted bit of ARINC 429 word (SDI)	None
49	BIT10	Digital Input	Data for 10th transmitted bit of ARINC 429 word (SDI)	None
50	BIT27	Digital Input	Data for 27th transmitted bit of ARINC 429 word	None
51	BIT28	Digital Input	Data for 28th transmitted bit of ARINC 429 word	None
52	BIT29	Digital Input	Data for 29th transmitted bit of ARINC 429 word	None
53	BIT30	Digital Input	Data for 30th transmitted bit of ARINC 429 word	None
54	BIT31	Digital Input	Data for 31st transmitted bit of ARINC 429 word	None
55	TMR7	Digital Input	Bit 7 of timer for automatic transmission interval selection	None
56	TMR6	Digital Input	Bit 6 of timer for automatic transmission interval selection	None
57	TMR5	Digital Input	Bit 5 of timer for automatic transmission interval selection	None
58	TMR4	Digital Input	Bit 4 of timer for automatic transmission interval selection	None
59	TMR3	Digital Input	Bit 3 of timer for automatic transmission interval selection	None
60	TMR2	Digital Input	Bit 2 of timer for automatic transmission interval selection	None
61	TMR1	Digital Input	Bit 1 of timer for automatic transmission interval selection	None
62	TMR0	Digital Input	Bit 0 of timer for automatic transmission interval selection	None
63	TXBDIG	Digital output	Logic level ARINC 429 negative signal for use with an external line driver	-
64	TXADIG	Digital output	Logic level ARINC 429 positive signal for use with an external line driver	-
65	GNDB	Supply	Lightning current return to Ground for the TXB output	-
66	TXB	Analog Output	ARINC 429 Line Driver negative output	-
67	TXA	Analog Output	ARINC 429 Line Driver positive output	-
68	GNDA	Supply	Lightning current return to Ground for the TXA output	-
69	TXENB	Digital Input	Enables automatic transmission or transmits on the positive edge	None
70	SEL0	Digital Input	If high Sense Channel 0 to be Supply/open, else GND/open	None
71	SEL1	Digital Input	If high Sense Channel 1 to be Supply/open, else GND/open	None
72	SEL2	Digital Input	If high Sense Channel 2 to be Supply/open, else GND/open	None
73	SEL3	Digital Input	If high Sense Channel 3 to be Supply/open, else GND/open	None
74	SEL4	Digital Input	If high Sense Channel 4 to be Supply/open, else GND/open	None
75	SEL5	Digital Input	If high Sense Channel 5 to be Supply/open, else GND/open	None
76	SEL6	Digital Input	If high Sense Channel 6 to be Supply/open, else GND/open	None
77	SEL7	Digital Input	If high Sense Channel 7 to be Supply/open, else GND/open	None
78	SEL8	Digital Input	If high Sense Channel 8 to be Supply/open, else GND/open	None
79	SEL9	Digital Input	If high Sense Channel 9 to be Supply/open, else GND/open	None
80	SEL10	Digital Input	If high Sense Channel 10 to be Supply/open, else GND/open	None
81	SEL11	Digital Input	If high Sense Channel 11 to be Supply/open, else GND/open	None
82	SEL12	Digital Input	If high Sense Channel 12 to be Supply/open, else GND/open	None
83	SEL13	Digital Input	If high Sense Channel 13 to be Supply/open, else GND/open	None
84	SEL14	Digital Input	If high Sense Channel 14 to be Supply/open, else GND/open	None
85	SEL15	Digital Input	If high Sense Channel 15 to be Supply/open, else GND/open	None
86	V-	Supply	If VDD=GND, attach a -6V supply, else a holding capacitor	-
87	CN+	Analog input	If VDD=GND, leave open, else a bucket capacitor plus side	-
88	CN-	Analog input	If VDD=GND, leave open, else a bucket capacitor minus side	-
89	GNDCONV	Supply	Converter and ARINC 429 Line Driver Ground	-
90	VDD	Supply	3.3V supply for DC/DC Converter and line Driver	-
91	CP-	Analog input	If VDD=GND, leave open, else a bucket capacitor minus side	-
92	CP+	Analog input	If VDD=GND, leave open, else a bucket capacitor plus side	-
93	V+	Supply	If VDD=GND, attach a +6V supply, else a holding capacitor	-

PIN DESCRIPTIONS

PIN	SYMBOL	FUNCTION	DESCRIPTION	PULL UP/DOWN
94	EXTTHSOG	Digital Input	If high selects THSLOOG and THSHIOG for GND/Open thresholds, else internal	30k pull-up
95	THSLOOG	Analog Input	Window comparator Low Threshold for GND/Open operation	-
96	THSHIOG	Analog Input	Window comparator High Threshold for GND/Open operation	-
97	EXTTHSVO	Digital Input	If high selects THSLOVG and THSHIVG for Supply/Open thresholds, else internal	30k pull-up
98	THSLOVO	Analog Input	Window comparator Low Threshold for Supply/Open operation	-
99	THSHIVO	Analog Input	Window comparator High Threshold for Supply/Open operation	-
100	VLOGIC	Supply	Digital Logic supply	-

PIN CONFIGURATION



100-pin Plastic Quad Flatpack (PQFP)

Figure 3

FUNCTIONAL DESCRIPTION

OVERVIEW

The HI-8470 has 16 Sense channels that are individually programmed for either GND/OPEN or SUPPLY/OPEN detection. The programming of each channel is set by strapping the appropriate SEL pin. There are 16 SENSE INPUT pins (SI15:0) with 16 corresponding SEL strap pins (SEL15:0).

The window comparator for detecting the state of the SENSE INPUT is offered with a choice of either standard internal voltage thresholds or, by option pins, the thresholds can be supplied externally. The choice of standard internal or external thresholds is selectable for each of the two sense functions, GND/OPEN and VOLTAGE/OPEN. If an external option is chosen, there are two pins for each function to input a HIGH or LOW level for thresholds. It is possible to set either of the external thresholds to logic levels such that a particular SEL option can function as digital state detection.

The HI-8470 has an onboard ARINC 429 transmitter. An on-chip DC-DC converter provides 3.3V-only operation, or external +6V and -6V power supplies may be connected. This selection is controlled by the voltage provided at the VDD pin.

The discrete sense pins and line driver outputs are lightning protected to RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B) without the use of any external components.

Logic and digital inputs and outputs operate from the VLOGIC supply.

A 1MHz clock must be provided at the CLKIN pin to operate the ARINC 429 transmitter. The Master Reset ($\overline{MR}$) pin is ORed with an on-chip Power On Reset (POR).

The SPEED pin selects the speed of the ARINC 429 transmission.

When set from logic 0 to logic 1, the TXENB input pin triggers ARINC 429 word transmission. The ARINC 429 transmitter is disabled when TXENB is held at logic 0. When TXENB is held at logic 1, periodic ARINC 429 word transmission occurs at a fixed interval programmed by eight input pins TMR7:0. When the TMR7:0 value ranges from 1 to 255 decimal, the word re-transmit interval equals TMR value x 10 milliseconds, or 10 to 2,550 ms.

Unique case:

When TMR7:0 equals zero, the ARINC 429 word re-transmission interval depends on the state of the SPEED input pin: For SPEED equals 0 (low-speed, 12.5kbit/s) the shortest interval is 2.88 ms when TMR7:0 equals 0. For SPEED equals 1 (high-speed, 100 kbit/s) the shortest re-transmission interval is 360 us when TMR7:0 equals 0.

After a detected Power On Reset, transmission is disabled for 500 ms to prevent spurious and possibly erroneous data.

The sense data for each of the 16 channels is transmitted directly in an ARINC 429 word. The label value is set by the eight Label input pins (LBL7:0). 2 pins (BIT9 and BIT10) configure the transmitted ARINC 429 SD bits. To allow additional flexibility, the last five bits of the ARINC 429 word are configured by the five BIT31:27 pins. Bits 11 through 26 of the ARINC 429 transmission have 16 bits of data mapped from the SENSE INPUT detections. The 32nd bit is odd parity. Note that the five bits of data set by the BIT31:27 pins could alternatively be used for detection and transmission of logic levels within the system.

Two pins (TEST1 and TEST0) provide a means of self test. If TEST0 is taken high, all comparator inputs are forced to ground and if TEST1 is taken high, all comparator inputs are forced high. If both self test inputs are high, the result is an alternating pattern with SI0 comparator input forcing a high input, Si1 forcing a ground input, etc.

FUNCTIONAL DESCRIPTION

SENSING

The 16 Sense Channels can be configured to meet the requirements of a variety of conditions and applications. Table 1 summarizes basic function selection and Table 2 gives more details on possible threshold values.

GND/OPEN SENSING

For GND/Open sensing, the channel's SEL pin is connected to GND. Referring to the Block Diagram, Figure 2, this selection will connect a 3.3kΩ pull-up resistor through a diode to VLOGIC and a 23.8kΩ resistor through 3 diodes to VWET. These resistors give extra noise immunity for detecting the open state while providing relay wetting current. Configuring EXTTHSOG, THSHIOG, THSLOOG and VWET as described below sets the window comparator thresholds, V_{THI} and V_{TLO}, the open input voltage when open, and the input current.

HI-8470 THRESHOLD SELECT

The HI-8470 offers a choice between internally fixed thresholds or external thresholds provided by the user.
With EXTTHSOG set to GND, the window comparator thresholds are fixed based on an internal reference. The high threshold, V_{THI}, and the low threshold, V_{THLO} levels may be found in Table 2. When the internal references are used the THSHIOG and THSLOOG pins should be connected to GND.
For applications with either large GND offsets or thresholds higher than VLOGIC - 0.75V, EXTTHSOG is set high and the thresholds are set externally, for example by a simple resistor divider off the VLOGIC supply. In this case V_{THI} is equal to 10X the voltage on the THSHIOG pin. V_{TLO} is equal to 10X the voltage on the THSLOOG pin. This mode allows the user complete flexibility to define the thresholds and hysteresis levels.

OPEN INPUT VOLTAGE

For correct operation, the V_{SENSE} when open, must be higher than V_{THI} so SO will be low. This condition requires VWET to be set greater than (VTHI/0.9 + 2.25V). Various ARINC standards such as ARINC 763 define the standard "Open" signal as characterized by a resistance of 100kΩ or more with respect to signal ground. The user should consider this 100kΩ to ground case when setting the thresholds.

WETTING CURRENT

For GND/Open applications with VWET open, the wetting current with the input voltage at GND is simply (VLOGIC - 0.75)/3.3k. When applying a higher voltage at the VWET pin the wetting current is (VLOGIC - 0.75)/3.3k + (VWET - 4.2)/127k. Additional wetting current can be achieved by placing an external resistor and a diode between VWET and the individual sense inputs.

SUPPLY/OPEN SENSING

The 16 Sense Channels can be individually configured to sense Supply/Open by connecting the channel's SEL pin to VLOGIC. Refering to Figure 2, a 32kΩ resistor is switched in series to provide a pull down in addition the 400kΩ of the comparator input divider to GND. Similar to the GND/Open case configuring EXTTHSVO, THSHIVO, THSLOVO and VWET as described below sets the window comparator thresholds, the open input voltage when open and the wetting current.

THRESHOLD SELECT

The threshold selections are handled in the same way as stated above for the GND/OPEN case.
For EXTTHSVO set low, the internal reference nominally sets the window comparator. See table 2 for the V_{THI} and V_{THLO} threshold levels.
For EXTTHSVO set high, again the final thresholds are 10X the voltage set on the THSHIVO and THSLOVO pins. The VWET pin is disconnected automatically when SEL is high.

WETTING CURRENT

For the Supply/Open case the wetting current into the sense input is the current sunk by the effective 28kΩ to GND. For V_{SENSE_n} = 28V, I_{WET} is 1ma. See Figure 4.

Table 1. Function Table

SI	SEL	SO
Open or > VTHI	L (GND/OPEN)	L
< VTLO	L (GND/OPEN)	H
Open or < VTLO	H (V+/OPEN)	H
> VThHI	H (V+/OPEN)	L
H = VLOGIC, L = GND, X = Don't Care, V+ = V_{SUPPLY} See Table 2 for values of VTHI/VTLO		

FUNCTIONAL DESCRIPTION

Table 2. Configuration options and allowed threshold values -55C to 125C.

VLOGIC	VWET Pin	Operation	Threshold Selected	Maximum HI_SET (VTHI = HI_SETx10)	Minimum LO_SET (VTLO = LO_SETx10)	Guaranteed High Threshold	Guaranteed Low Threshold
3.0V	OPEN	GND/OPEN	Internal	-	-	2.5V	0.8V
3.6V	OPEN	GND/OPEN	Internal	-	-	2.7V	0.8V
3.3V	28V	GND/OPEN	Internal	-	-	2.55V	0.8V
3.0V to 3.6V	7V	GND/OPEN	External	0.4V (4.0V)	0.3V (3.0V)	VTHI + 0.5V	VTLO - 0.5V
3.0V to 3.6V	28V	GND/OPEN	External	2.2V (22V)	0.3V (3.0V)	VTHI + 0.5V	VTLO - 0.5V
3.0V to 3.6V	OPEN	V+/OPEN	Internal	-	-	15.5V	11.0V
3.0V to 3.6V	OPEN	V+/OPEN	Exernal	2.2V (22V)	0.3V (3.0V)	VTHI + 0.5V	VTLO - 0.5V

NOTE: VTHI = Sense pin high threshold (HI_SET x 10), VTLO = Sense pin low threshold (LO_SET x 10)

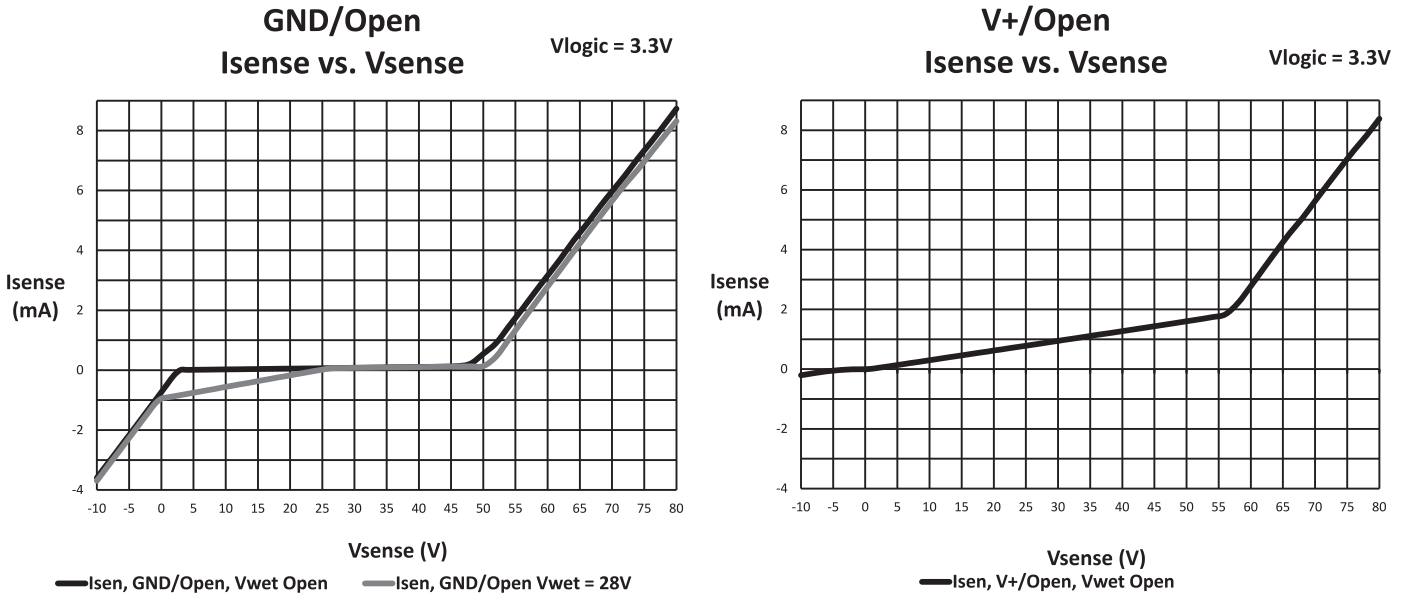


Figure 4 Input Current Vs. Input Voltage

FUNCTIONAL DESCRIPTION

ARINC 429 TRANSMITTER

ARINC 429 WORD ASSEMBLY

ARINC 429 words transmitted by the HI-8470 are formatted as shown in Figure 5. The first eight bits transmitted are the ARINC 429 label byte. The label value reflects the state of pins LBL7 through LBL0 immediately prior to transmission. ARINC 429 SD bits (bits 9 and 10) reflect the state of the BIT9 and BIT10 pins immediately prior to transmission. The next 19 bits comprise a discrete data field as defined in ARINC Specification 429 Part 1, Attachment 6 “Discrete word format”. Bits 11 through 26 reflect the state of discrete sense pins SI0 through SI15 respectively, and bits 28 and 29 reflect the state of the BIT28 and BIT29 pins. The ARINC 429 SSM bits, bit 30 and 31 are set by input pins BIT30 and BIT31. The last transmitted ARINC 429 bit is an odd parity bit, which is automatically calculated by the HI-8470.

ARINC 429 BIT RATE

A 1 MHZ clock signal must be provided at the CLKIN input pin. This clock provides the timing reference for the ARINC 429 transmitter and word scheduler.

The SPEED input pin sets the ARINC 429 transmission bit rate and line driver slope control. When SPEED is high the transmitter is set for ARINC 429 high-speed bit rate of 100 kbit/s and the line driver differential rise and fall time is set to 1.5 us. When SPEED is low, the bit rate is 12.5 kbit/s and the line driver differential rise and fall time is nominally 10

ARINC 429 TRANSMITION SCHEDULING

The HI-8470 outputs ARINC 429 words under the control of the TXENB and TMR7:0 pins. Words may be output in single-shot mode or periodically.

If TXENB is held low, no ARINC 429 words are transmitted. Pulsing TXENB high for 1-2 us causes transmission of a single ARINC 429 word. When TXENB is held high, the ARINC 429 words are transmitted at a periodic interval determined by the eight TMR pins. If all TMR pins are low, the HI-8470 transmits words at the maximum possible rate allowed by the ARINC 429 specification. That time is equal to 36 bit periods (32 data bits plus 4 gap times). For high speed ARINC 429 (SPEED=1), the word interval is 360 us, and for low-speed ARINC 429 (SPEED=0), the word interval is 2.88 ms.

Table 5 describes TXENB function for all cases of TXENB pulse widths and periods.

The word transmission interval may be increased in 10 ms steps by setting the TMR7:0 to a non zero value. The transmission interval is given by t = TMR7:0 x 10 ms except when TMR7:0 equals 0. Example transmission intervals are shown in Table 6.

TXENB Action	Pulse width	Result
TXENB wired High	Infinite	First transmit after POR period finished and programmed intervals thereafter
TXENB goes high	Less than interval programmed	Transmit on positive edge only
TXENB goes high	More than interval time	Transmit on positive edge and on each interval completion at which TXENB remains high
TXENB goes high twice during transmit	Two pulses such that second edge comes before ARINC word transmitted	Transmit on first positive edge Ignore second pulse edge and transmit again only if TXENB remains high to interval completion The interval is reset any time TXENB is low and starts again when TXENB goes high
TXENB goes high twice during interval	Pulse spacing wider than ARINC word	Transmit each edge and restart interval timer each edge

Table 5. TXENB Function Description

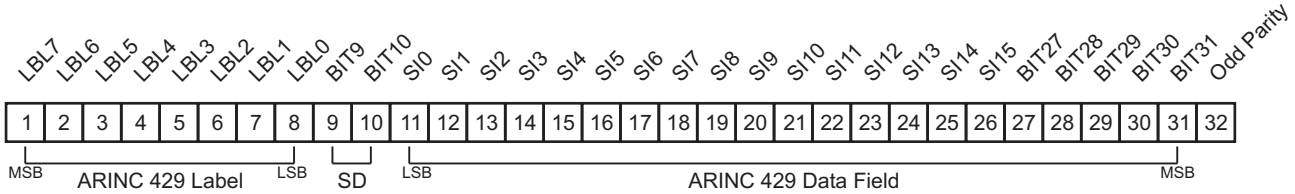


Figure 5. ARINC 429 Word Format

FUNCTIONAL DESCRIPTION

ARINC 429 LINE DRIVER

The HI-8470 includes a 3.3V single supply ARINC 429 line driver. Internal lightning protection circuitry complies with RTCA/DO-160 Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B) without external components. Pin surge levels for Level 3 are summarized as follows:

Waveform 3	Waveform 4	Waveform 5A	Waveform 5B
VOC/ISC 600V/24A	VOC/ISC 300V/60A	VOC/ISC 300V/300A	VOC/ISC 300V/300A

The waveforms are shown in Figure 6.

An internal 37.5 Ohm resistor on each output enables direct connection to the ARINC 429 bus.

The line driver requires only a single 3.3V power supply. An integrated inverting / non-inverting voltage doubler generates the rail voltages (+/- 6.6V) which are then used to produce the +/-5V ARINC 429 output levels.

The internal dual-polarity charge pump circuit requires four external capacitors, two capacitors for each polarity. CP+ and CP- connect the external charge transfer or “fly” capacitor, CFLY, to the positive portion of the doubler, resulting in twice VDD at the V+ pin. An output “hold” capacitor, COUT, is placed between V+ and GND. COUT should be ten times the size of CFLY. The inverting or negative portion of the converter works in a similar fashion, with CFLY and COUT placed between CN+/CN- and V-/GND respectively.

Currents for output slope control are set by on-chip resistors. The charging current is selected by the SPEED pin. If SPEED is high, the output rise/fall time 10% to 90% is 1.5us. If SPEED is low, the rise and fall times are 10us.

A unity gain buffer receives the internally generated slopes and differentially drives the ARINC line. Current is limited by the series output resistors at each pin. There are no fuses at the outputs of the HI-8470.

The HI-8470 has 37.5 Ohms in series with the TXA and TXB outputs, allowing direct connection to the ARINC 429 bus. The outputs are automatically lightning protected in compliance with RTCA/DO-160G, Section 22 Lavel 3 Pin Injection Test Waveform Set A (3 &4), Set B (3 &5A) and Set Z (3 & 5B) without any external components.

The HI-8470 may also be used with an external line driver, for example when designing a system for DO-160G level 4 or higher lightning protection. The two digital outputs directly drive the digital inputs of any stand-alone Holt ARINC 429 line driver, such as the HI-8592 or HI-8596.

SPEED	TMR7:0	BIT RATE	SLOPE	REPETITION INTERVAL	WORDS/ SECOND
0	0x00	12.5 kbit/s	10 us	2.88 ms	347.2
1	0x00	100 kbit/s	1.5 us	360 us	2,777
X	0x01	X	X	10 ms	100
X	0x05	X	X	50 ms	20
X	0x0A	X	X	100 ms	10
X	0x14	X	X	200 ms	5
X	0x32	X	X	500 ms	2
X	0x64	X	X	1 s	1
X	0xC8	X	X	2 s	0.5
X	0xFF	X	X	2.55 s	0.392
X = Don’t Care					

Table 6. Example Transmission Schedule Rates

LIGHTNING PROTECTION

The discrete sense pins and line driver outputs are lightning protected to RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B) without the use of any external components. Figures 5, 6 and 7 summarize the waveforms.

Waveform 3

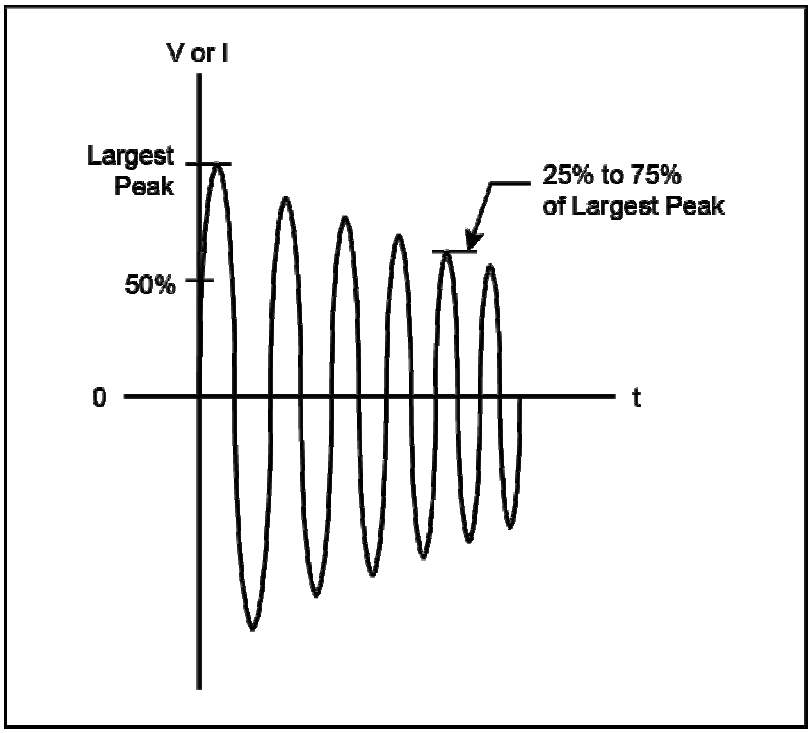


Figure 5. DO-160G Lightning Induced Transient Voltage Waveform 3. Voc = 600V, Isc = 24A, Frequency = 1MHz ± 20%.

Waveform 4

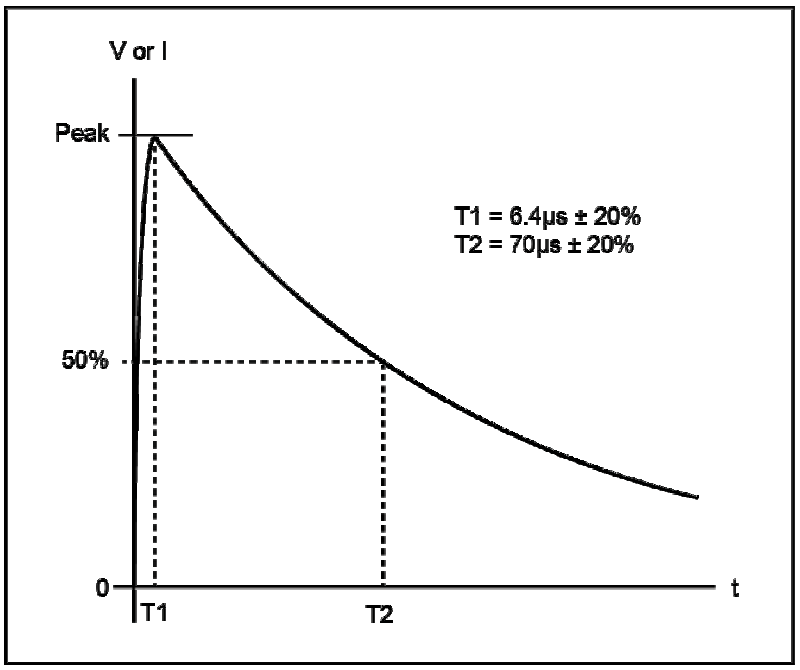


Figure 6. DO-160G Lightning Induced Transient Voltage Waveform 4.
Voc = 300V, Isc = 60A.

Waveform 5

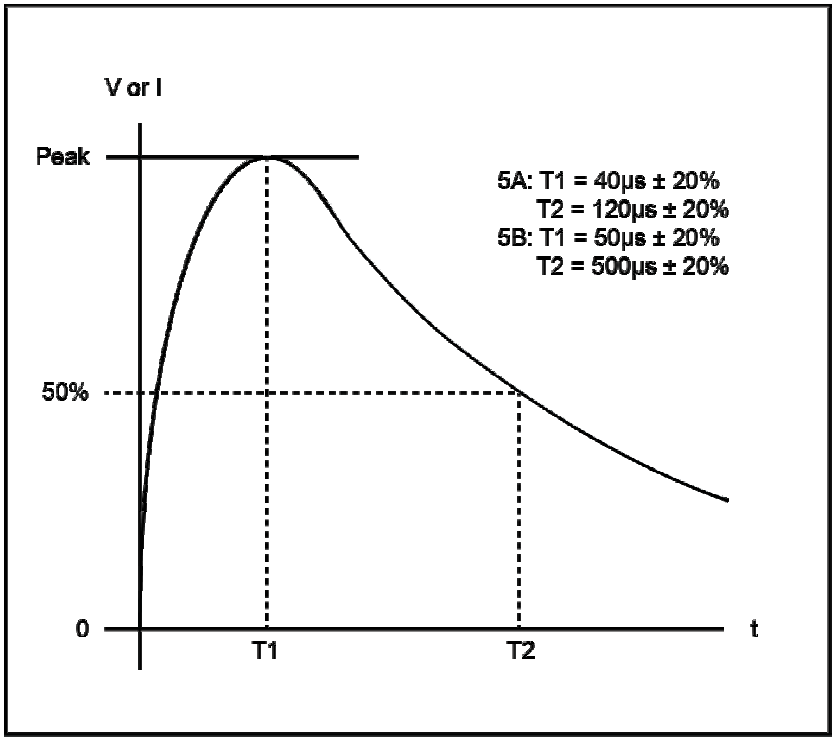


Figure 6. DO-160G Lightning Induced Transient Voltage Waveforms 5A and 5B.
Voc = 300V, Isc = 300A.

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to Ground	
Supply Voltage (VLOGIC)	-0.3V to +7V
VWET	-0.3V to +50V
Max. DC Current at any pin	125mA
Logic Input Voltage Range	-0.3V to VLOGIC+0.3V
Discrete Input Voltage Range	-50V to +50V
Continuous Power Dissipation (TA=+70°C) QFN (derate 21.3mW/°C above +70°C) QFP (derate 10.0mW/°C above +70°C)	 1.7W 1.5W
Solder Temperature (reflow)	260°C
Junction Temperature	175°C
Storage Temperature	-65°C to -150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	
VLOGIC	3.0V to 3.6V
VWET	7.0V to 36V
Operating Temperature Range	
Industrial Screening	-40°C to +85°C
Hi-Temp Screening	-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

D.C. ELECTRICAL CHARACTERISTICS

VDD = VLOGIC = 3.3V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
DISCRETE INPUTS						
SENSE V+/OPEN		SEL_n = High				
Resistance to Ground	R_{IN}			30		kΩ
Case 1: EXTTHSVO = GND		Internal Threshold Mode				
Open State Input Voltage	V_{OS}	Input voltage to give High output			11.0	V
V+ State Input Voltage	V_{V+}	Input voltage to give Low output	15.5			V
Open State Input Current	I_{OS}	Max input current to give High output			325	µA
V+ State Input Current	I_{V+}	Min Input current to give Low output	640			µA
Input Current at 36V	I_{IN28}	V_{IN} = 36V		1.0		mA
Hysteresis	V_{HY}		1.5			V
Case 2: EXTTHSVO = Open or VLOGIC		THSHIVO/THSLOVO set Thresholds				
THSHIVG Threshold Range	V_{HR}	HI Threshold is set to THSHIHG X 10	0.4		2.2	V
THSLOVG Threshold Range	V_{LR}	LO Threshold is set to THSLOVO X10	0.3		2.1	V
Min Threshold Window	V_{THW}	THSHIVO > THSLOVO	0.1			V
10:1 Division Accuracy		As measured by Sense Output Change	V_{LR} - 0.5		V_{HR} + 0.5	V

D.C. ELECTRICAL CHARACTERISTICS (cont)

VDD = VLOGIC = 3.3V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
DISCRETE INPUTS						
SENSE GND/OPEN						
Resistance in series with diode to VLOGIC	R_{IN}			3.3		kΩ
Resistance in series with diode to VWET	R_W			23.8		kΩ
Case 1: EXTTHSOG = GND		Internal Threshold Mode				
Ground State Input Voltage	V_{GS}	Input voltage to give High output			0.8	V
Open State Input Voltage	V_{OS}	Input voltage to give Low output VDD = 3.0V	2.5			V
Input Current at 0V	I_{IN28}	V_{IN} = 0V, VDD = 3.0V		-0.65		mA
Hysteresis	V_{HY}		0.15			V
Case 2: EXTTHSOG = Open or VLOGIC		THSHIOG/THSLOOG pins set Thresholds				
THSHIOG Threshold Range	V_{HR}	HI Threshold is set to THSHIOG X 10	0.4		2.2	V
THSLOOG Threshold Range	V_{LR}	LO Threshold is set to THSLOOG X 10	0.3		2.2	V
Min Threshold Window	V_{THW}	THSHIOG > THSLOOG	0.1			V
10:1 Division Accuracy		As measured by Sense Output Change	V_{LR} - 0.5		V_{HR} + 0.5	V
LOGIC INPUTS						
Input Voltage	V_{IH}	Input Voltage HI	80%			VLOGIC
	V_{IL}	Input Votage LO			20%	VLOGIC
Input Current, TEST0, TEST1	I_{SINK}	V_{IN} = VLOGIC, 30kΩ pull down		125		µA
	I_{SOURCE}	V_{IN} = GND			0.1	µA
Input Current, $\overline{MR}$, EXTTHSOG, EXTTHSVG	I_{SINK}	V_{IN} = VLOGIC	0.1			µA
	I_{SOURCE}	V_{IN} = GND , 30kΩ pull up		125		µA
Input Current (all other logic inputs)	I_{SINK}	V_{IN} = VLOGIC	0.1			µA
	I_{SOURCE}	V_{IN} = GND,	0.1			µA
LOGIC OUTPUTS						
Output Voltage	V_{OH}	I_{OH} = -100µA	90%			VLOGIC
	V_{OL}	I_{OL} = 100µA			10%	VLOGIC
Output Current	I_{OL}	V_{OUT}= 0.4V	1.6			mA
	I_{OH}	V_{OUT} = VLOGIC - 0.4V			-1.0	mA
Output Capacitance	C_O			15		pF

D.C. ELECTRICAL CHARACTERISTICS (cont)

VDD = VLOGIC = 3.3V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
ANALOG INPUTS						
THSHI/THSLO Leakage Current	I_L	Max leakage for VLOGIC > V_{input} > GND	-0.1		1.0	µA
LINE DRIVER OUTPUTS						
ARINC 429 Output Voltage (Differential) One Zero Null	 V_{DIFF1} V_{DIFF1} V_{DIFF1}	No load; TXA - TXB	 9 -11 -0.5	 10 -10 0	 11 -9 0.5	 V V V
ARINC 429 Output Voltage (Ref. to GND) One or Zero Null	 V_{DOUT} V_{NOUT}	 No load & magnitude at pin No load	 4.5 -0.25	 5.0 0	 5.5 0.25	 V V
ARINC 429 Output Impedance TXA, TXB pins	 Z_{OUT}			 37.5		 Ω
DC/DC CONVERTER CHARACTERISTICS						
Start-up transient (V+, V-)	t_{START}		-	-	10	ms
Operating Switching Frequency	f_{SW}		-	650	-	kHz
Worst-case maximum voltage doubler output	$V+_{(MAX)}$	VDD = 3.6V. T=-55°C. Open load.	-	-	6.93	V
Ratio of bulk storage to fly-back capacitors	C_{OUT}/C_{FLY}		2.2			
Fly-back capacitor (Recommend multilayer ceramic, dielectric XR7 caps, 10V min)	C_{FLY} $C_{FLY(ESR)}$	C_{OUT}/C_{FLY} >=10 [0.5,1.0]MHz	1.0 500	4.7		µF mΩ
Bulk storage capacitor (Recommend multilayer ceramic, dielectric XR7 caps, 10V min)	C_{OUT} $C_{OUT(ESR)}$	C_{OUT}/C_{FLY} >=10 [0.5,1.0]MHz	2.2 300	47		µF mΩ
Bypass capacitor ESR 100mΩ max. (Recommend tantalum cap, 10V min)	C_{SUPPLY}	C_{SUPPLY}>=C (connect from VDD to GND)	47			µF
SUPPLY						
VDD Supply current No load Max load (400Ω)	 I_{DDNL} I_{DDL}	SPEED = 1 Continuous transmission, TMR7:0 = 0		 28 65	40	 mA mA
Operating VLOGIC range	VLOGIC		3.0		3.6	V
Operation VWET range	VWET		0		28	V
VLOGIC Current	I_{DD1}	All Sense Pins Open			10	mA
VWET Current	I_{VWET}	All Sense Inputs = 0V, VWET = 28V			30	mA

AC ELECTRICAL CHARACTERISTICS

VDD = 3.3V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
SENSE V+/OPEN						
Delay, Output going High	t_{H1}			1.0		µs
Delay, Output going Low	t_{L1}			1.0		µs
SENSE GND/OPEN						
Delay, Output going High	t_{H2}			1.0		µs
Delay, Output going Low	t_{L2}			1.0		µs
LINE DRIVER						
Line Driver Transistion Times						
High Speed (SPEED = 1)						
Output high to low	t_{FX1}		1.0	1.5	2.0	µs
Output low to high	t_{RX1}		1.0	1.5	2.0	µs
Low Speed (SPEED = 0)						
Output high to low	t_{FX2}		5.0	10.0	15.0	µs
Output low to high	t_{RX2}		5.0	10.0	15.0	µs
CLOCK (CLKIN)						
Clock frequency for ARINC 429 compliance	f_{CLKIN}			1.0 +/- 1%		MHZ

ORDERING INFORMATION

HI - 8470PQ x F

PART NUMBER	LEAD FINISH
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO

PART NUMBER	PACKAGE DESCRIPTION
8470PQ	100 PIN PLASTIC QUAD FLATPACK (100PQS)

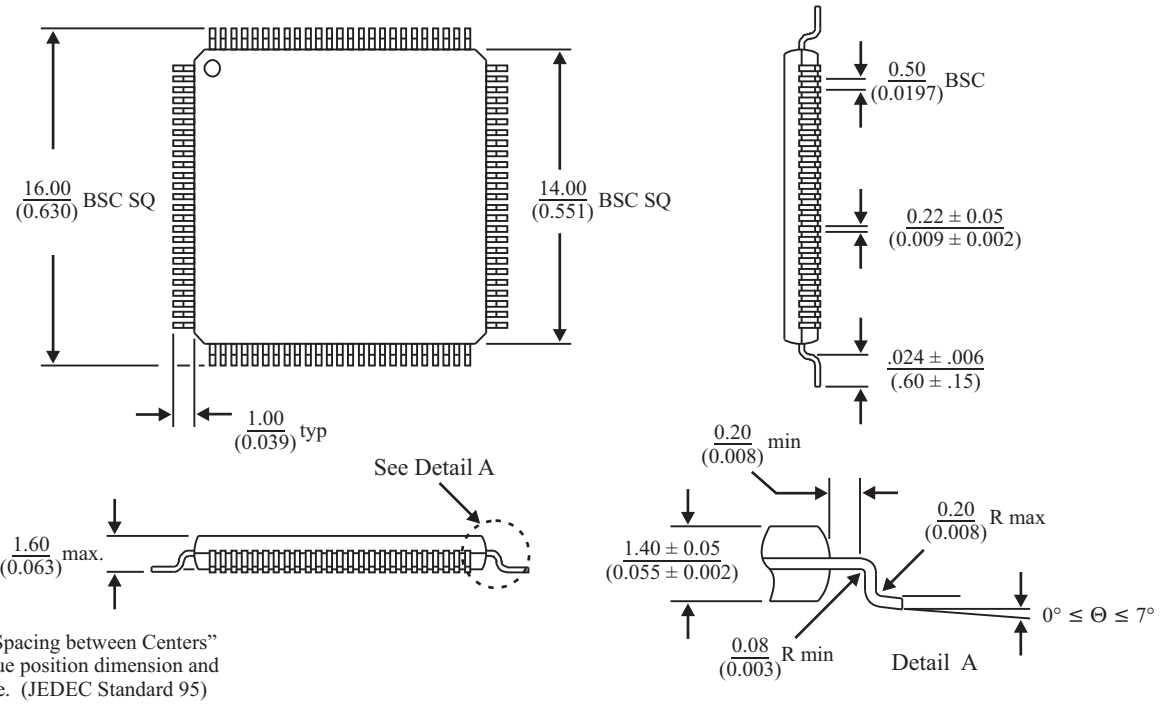
REVISION HISTORY

P/N	Rev	Date	Description of Change
DS8470	A	5/31/13	Changed maximum ground state input voltage for ground detection from 1.0V to 0.8V. Corrected typo for V+ state input voltage in DC Characteristics from 15.0V to 15.5V. Changed maximum wetting current from 20mA to 30mA.
	B	10/10/13	Corrected error in block diagram.
	C	01/12/15	Correct typo in Pin Descriptions of TXADIG and TXBDIG pins (negative and positive reversed). Update 100PQS package. Correct minor typos. Clarify Input Current for Logic Inputs in DC Electrical Characteristics.

100-PIN PLASTIC QUAD FLAT PACK (PQFP)

millimeters (inches)

Package Type: 100PQS



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)