HOLT INTEGRATED CIRCUITS INC.

HI-8444, HI-8445, HI-8448

Quad / Octal ARINC 429 Line Receivers

November 2013

DESCRIPTION

The HI-8444 and HI-8445 are quad ARINC 429 line receiver ICs available in a 20-pin TSSOP package. The HI-8448 contains 8 independent ARINC 429 line receivers. The technology is analog / digital CMOS. The device is designed to operate from either a 5V or 3.3V supply. Each receiver channel translates incoming ARINC 429 data bus signals to a pair of TTL / CMOS outputs.

The optional HI-8444-10, HI-8445-10 and HI-8448-10 are designed to be used with an external 15 Kohm series resistor. The "-10" devices meet the lightning protection requirements of DO-160G, level 3, waveforms 3, 4, 5A, and 5B.

The TESTA and TESTB inputs bypass the analog inputs for testing purposes. They force the receiver outputs to the specified ZERO, ONE or NULL state. The ARINC inputs are ignored when the device is in the test mode.

The HI-8445 is identical to the HI-8444 except the TESTA and TESTB pins are not available.

FEATURES

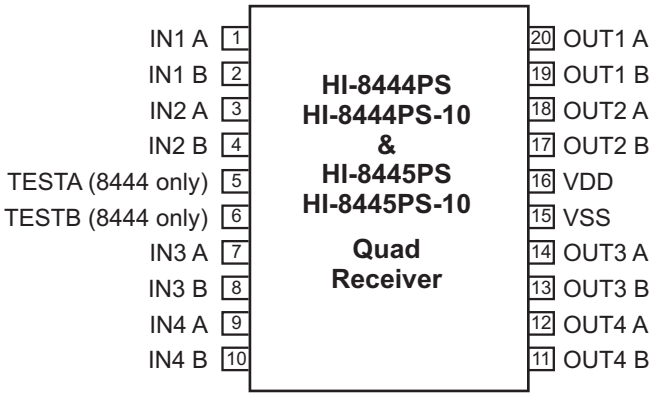
- Direct ARINC 429 quad or octal line receivers in small footprint packages
- 3.3V or 5.0V single supply operation
- Test inputs bypass analog inputs and force digital outputs to a one, zero, or null state
- ARINC inputs are internally lightning protected per DO-160G level 3 (-10 configuration only)
- Hi-Rel processing options available

FUNCTION TABLE

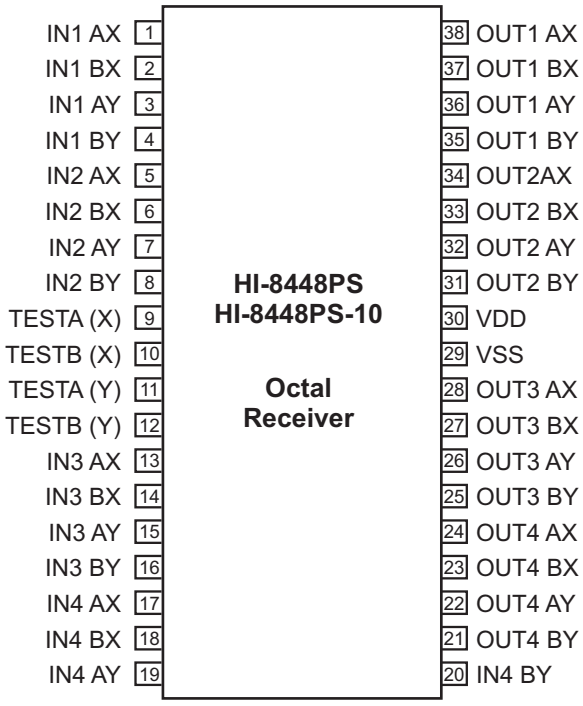
ARINC INPUTS INA - INB	TESTA	TESTB	OUTA	OUTB
-2.5 to +2.5 V	0	0	0	0
< -6.5 V	0	0	0	1
> +6.5 V	0	0	1	0
X	0	1	0	1
X	1	0	1	0
X	1	1	0	0

PIN CONFIGURATIONS

(See page 6 for additional pin configurations)

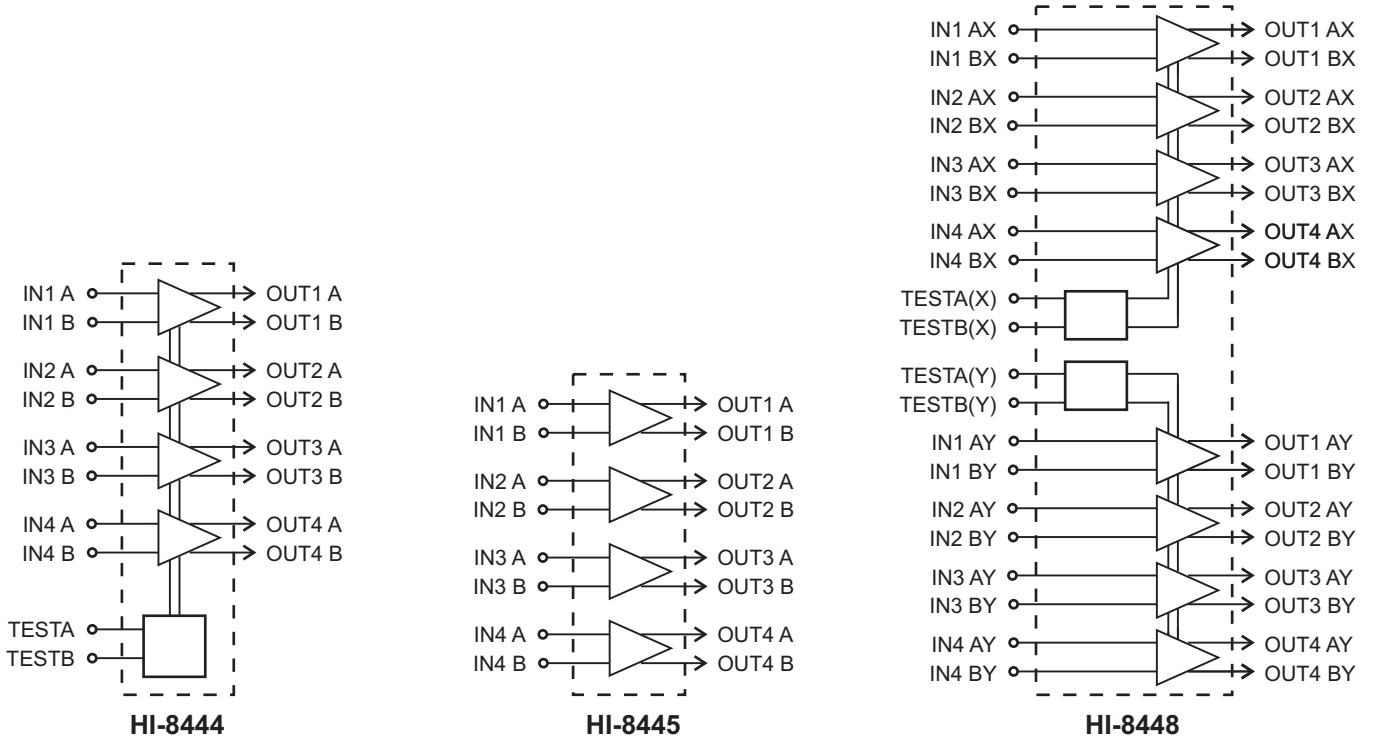


20 Pin Plastic TSSOP package



38 Pin Plastic TSSOP package

BLOCK DIAGRAMS



PIN DESCRIPTIONS (HI-8444, HI-8445)

PIN	SYMBOL	FUNCTION	DESCRIPTION
1	IN1 A	ARINC input	Receiver 1 positive input
2	IN1 B	ARINC input	Receiver 1 negative input
3	IN2 A	ARINC input	Receiver 2 positive input
4	IN2 B	ARINC input	Receiver 2 negative input
5	TESTA	Logic input	Test input. (Not available on HI-8445)
6	TESTB	Logic input	Test input. (Not available on HI-8445)
7	IN3 A	ARINC input	Receiver 3 positive input
8	IN3 B	ARINC input	Receiver 3 negative input
9	IN4 A	ARINC input	Receiver 4 positive input
10	IN4 B	ARINC input	Receiver 4 negative input
11	OUT4 B	Logic output	Receiver 4 "ZERO" output
12	OUT4 A	Logic output	Receiver 4 "ONE" output
13	OUT3 B	Logic output	Receiver 3 "ZERO" output
14	OUT3 A	Logic output	Receiver 3 "ONE" output
15	VSS	Power	Ground
16	VDD	Power	Positive supply voltage 3.3V or 5.0 V
17	OUT2 B	Logic output	Receiver 2 "ZERO" output
18	OUT2 A	Logic output	Receiver 2 "ONE" output
19	OUT1 B	Logic output	Receiver 1 "ZERO" output
20	OUT1 A	Logic output	Receiver 1 "ONE" output

PIN DESCRIPTIONS (HI-8448)

PIN	FUNCTION	RECEIVER SET	DESCRIPTION
IN1 AX	ARINC input	X	Receiver 1 positive input
IN1 BX	ARINC input	X	Receiver 1 negative input
IN1 AY	ARINC input	Y	Receiver 1 positive input
IN1 BY	ARINC input	Y	Receiver 1 negative input
IN2 AX	ARINC input	X	Receiver 2 positive input
IN2 BX	ARINC input	X	Receiver 2 negative input
IN2 AY	ARINC input	Y	Receiver 2 positive input
IN2 BY	ARINC input	Y	Receiver 2 negative input
TESTA(X)	Logic input	X	Test input
TESTB(X)	Logic input	X	Test input
TESTA(Y)	Logic input	Y	Test input
TESTB(Y)	Logic input	Y	Test input
IN3 AX	ARINC input	X	Receiver 3 positive input
IN3 BX	ARINC input	X	Receiver 3 negative input
IN3 AY	ARINC input	Y	Receiver 3 positive input
IN3 BY	ARINC input	Y	Receiver 3 negative input
IN4 AX	ARINC input	X	Receiver 4 positive input
IN4 BX	ARINC input	X	Receiver 4 negative input
IN4 AY	ARINC input	Y	Receiver 4 positive input
IN4 BY	ARINC input	Y	Receiver 4 negative input
OUT4 BY	Logic output	Y	Receiver 4 "ZERO" output
OUT4 AY	Logic output	Y	Receiver 4 "ONE" output
OUT4 BX	Logic output	X	Receiver 4 "ZERO" output
OUT4 AX	Logic output	X	Receiver 4 "ONE" output
OUT3 BY	Logic output	Y	Receiver 3 "ZERO" output
OUT3 AY	Logic output	Y	Receiver 3 "ONE" output
OUT3 BX	Logic output	X	Receiver 3 "ZERO" output
OUT3 AX	Logic output	X	Receiver 3 "ONE" output
VSS	Power		Ground supply
VDD	Power		Positive supply voltage 3.3V or 5.0 V
OUT2 BY	Logic output	Y	Receiver 2 "ZERO" output
OUT2 AY	Logic output	Y	Receiver 2 "ONE" output
OUT2 BX	Logic output	X	Receiver 2 "ZERO" output
OUT2 AX	Logic output	X	Receiver 2 "ONE" output
OUT1 BY	Logic output	Y	Receiver 1 "ZERO" output
OUT1 AY	Logic output	Y	Receiver 1 "ONE" output
OUT1 BX	Logic output	X	Receiver 1 "ZERO" output
OUT1 AX	Logic output	X	Receiver 1 "ONE" output

ABSOLUTE MAXIMUM RATINGS

Supply voltage (VDD)	-0.3 V to +7 V
Logic input voltage range	-0.3 V to +5.5 V
ARINC input voltage	-120 V to + 120 V
Driver peak output current	+1.0 A
Power dissipation at 25°C	350 mW
Solder Temperature	275°C for 10 sec
Storage Temperature	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	
VDD	3.0 V to 5.5 V
Operating Temperature Range	
Industrial Screening	-40°C to +85°C
Hi-Temp Screening	-55°C to +125°C

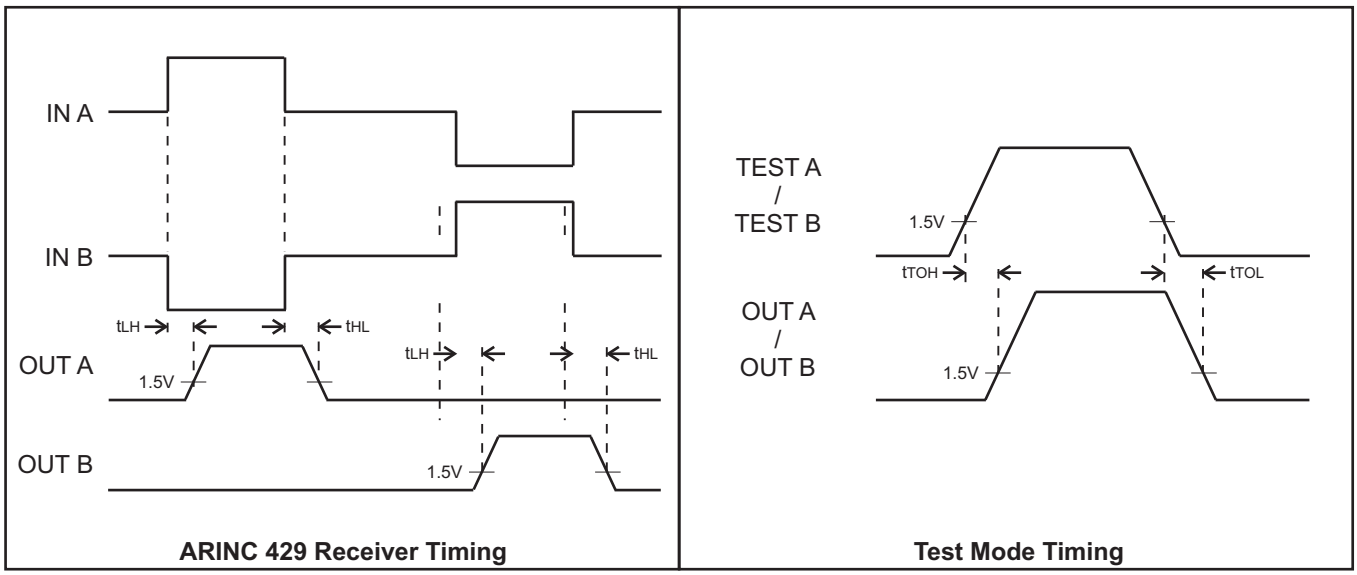
NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

ELECTRICAL CHARACTERISTICS

VDD = 5.0V ± 5% or 3.3V ± 5%, V_{SS} = 0V, T_A = Operating Temperature Range (unless or otherwise specified).

PARAMETER		SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
ARINC INPUTS							
Input voltage	ONE or ZERO	V_{DIN}	Differential input voltage	6.5	10	13	V
	NULL	V_{NIN}	Differential input voltage			2.5	V
	Common mode	V_{COM}	With respect to GND			±5.0	V
Input resistance	INA to INB	R_{DIFF}	Supplies floating	30	75		KΩ
	Input to V_{SS} or V_{DD}	R_{SUP}	Supplies floating	19	40		KΩ
Input hysteresis		V_{HYS}		0.5	1.0		V
Input capacitance	ARINC differential	C_{AD}			5	10	pF
	ARINC single ended to V_{SS}	C_{AS}				10	pF
TEST INPUTS							
Logic input voltage	High	V_{IH}		2.0			V
	Low	V_{IL}				0.8	V
Logic input current	Sink	I_{IH}	V_{IH}=2.0V			200	µA
	Source	I_{IL}	V_{IL}=0.8V	-1.0			µA
OUTPUTS							
Logic output voltage	High	V_{OH}	I_{OH}=-5mA, V_{DD}=5.0V	2.4			V
			I_{OH}=-4mA, V_{DD}=3.3V	2.4			V
	Low	V_{OL}	I_{OL}=5mA, V_{DD}=5.0V			0.4	V
			I_{OL}=4mA, V_{DD}=3.3V			0.4	V
Logic output voltage (CMOS)	High	V_{OHC}	I_{OH}=-100µA	V_{DD}-0.2			V
	Low	V_{OLC}	I_{OL}=100µA			V_{SS}+0.2	V
SUPPLY CURRENT							
V_{DD} current		I_{DD}	HI-8444, HI-8445		5.5	10	mA
			HI-8448		11	20.0	mA
SWITCHING CHARACTERISTICS (T_A = 25 °C)							
Propagation delay	IN to OUT	t_{LH}	C_L=50 pF		600		ns
		t_{HL}	C_L=50 pF		600		ns
Output rise time		t_R	10% to 90%		50	80	ns
Output fall time		t_F	90% to 10%		50	80	ns
Propagation delay	TEST to OUT	t_{TOH}			50		ns
		t_{TOL}			50		ns

TIMING DIAGRAMS



ARINC 429 Receiver Timing | **Test Mode Timing**

INTERNAL LIGHTNING PROTECTION (-10 Only)

The HI-8444-10, HI-8445-10 and HI-8488-10 are similar to the "non -10" configurations with the exception that an external 15 Kohm resistor must be added in series with each ARINC input in order to properly detect the ARINC 429 specified input thresholds. This option is especially useful in applications where external lightning protection circuitry is required.

The HI-8444-10, HI-8445-10 and HI-8448-10 will meet the requirements of DO-160G, Level 3, waveforms 3, 4, 5A and 5B with the 15 Kohm series resistors in place.

Please refer to the Holt AN-300 Application Note for additional information and recommendations on lightening protection of Holt Line Drivers and Receivers.

ORDERING INFORMATION

HI - 844xxx x x - xx

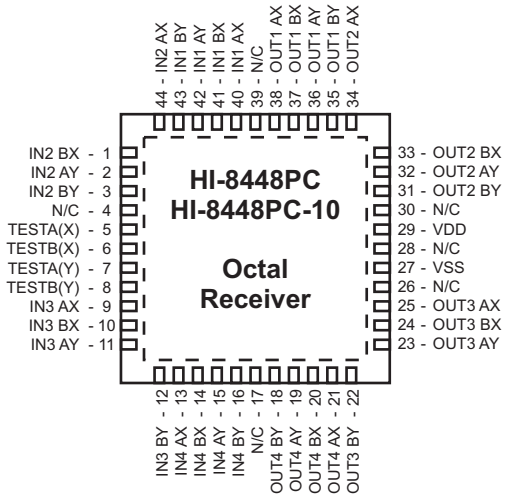
PART NUMBER	INPUT SERIES RESISTANCE	
	BUILT-IN	REQUIRED EXTERNALLY
No dash number	35 Kohm	0
-10	25 Kohm	15 Kohm

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

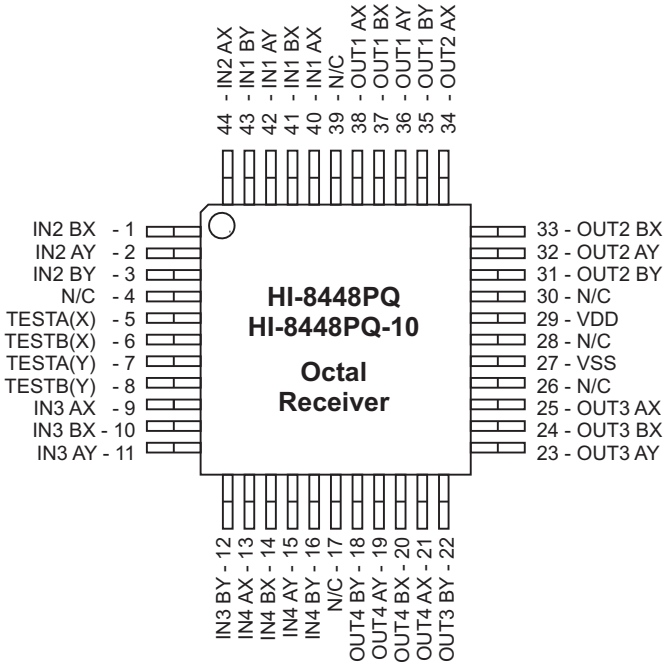
PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No

PART NUMBER	PACKAGE DESCRIPTION	TEST PINS
8444PS	20 PIN PLASTIC TSSOP (20HS)	Yes
8445PS	20 PIN PLASTIC TSSOP (20HS)	No
8448PQ	44 PIN PLASTIC QUAD FLAT PACK PQFP (44PTQS)	Yes
8448PS	38 PIN PLASTIC TSSOP (38HS)	Yes
8448PC	44 PIN PLASTIC CHIP-SCALE, LPCC (44PCS)	Yes

ADDITIONAL PIN CONFIGURATIONS



44 - Pin Plastic 7mm x 7mm Chip-Scale Package (QFN)



44-Pin Plastic Quad Flat Pack (PQFP)

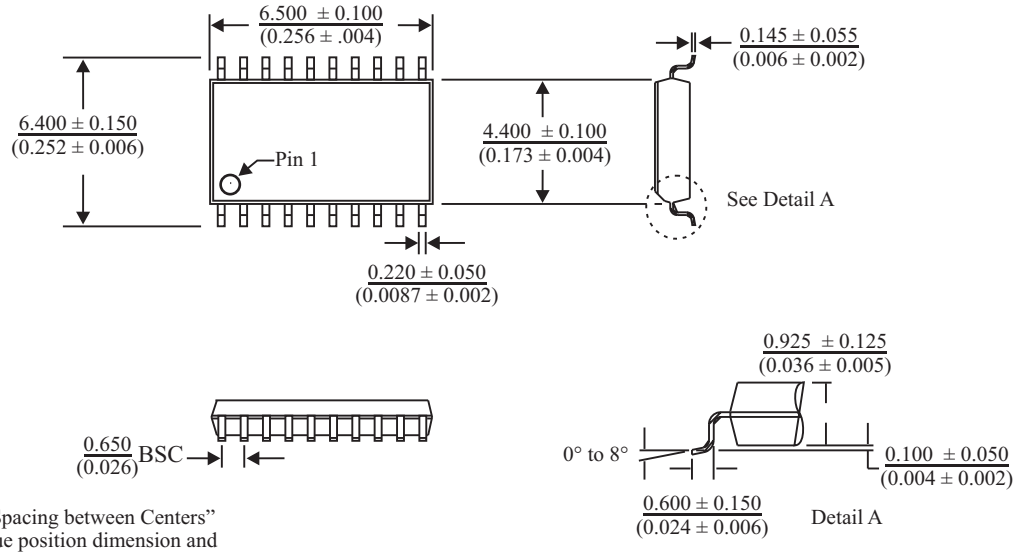
REVISION HISTORY

Revision	Date	Page	Description of Change
DS8444, Rev. G	05/30/08	1	Changed “10 Kohm”, “DO-160C/D”, and “and 5A” in second paragraph of the Description to “15 Kohm”, DO-160E”, and “5A, and 5B” respectively.
		1	Changed “DO-160C/D” in fourth Feature bullet to “DO160E”.
		5	Changed “10 Kohm” in second and third paragraphs and in the Required Series Resistance of the Ordering information to “15 Kohm”.
		5	Changed “DO-160D” and “4 and 5A” in third paragraph to “DO-160E” and “4, 5A, and 5B” respectively.
		6	Added Revision History page as new page 6.
		7	Renumbered page 6 as page 7
		8	Replaced the 44-Pin Plastic Quad Flat Pack (PQFP) drawing with new drawing.
Rev. H	05/25/10		Added new package configurations for HI-8448PSx and HI-8448PCx.
Rev. I	10/17/13		Update PQFP and QFN package drawings.
Rev. J	11/04/13		Update QFN-44, QFP-44, TSSOP-38 and TSSOP-20 package drawings. Update DO-160E to DO-160G rev. number in text.

20-PIN PLASTIC TSSOP

millimeters(inches)

Package Type: 20HS

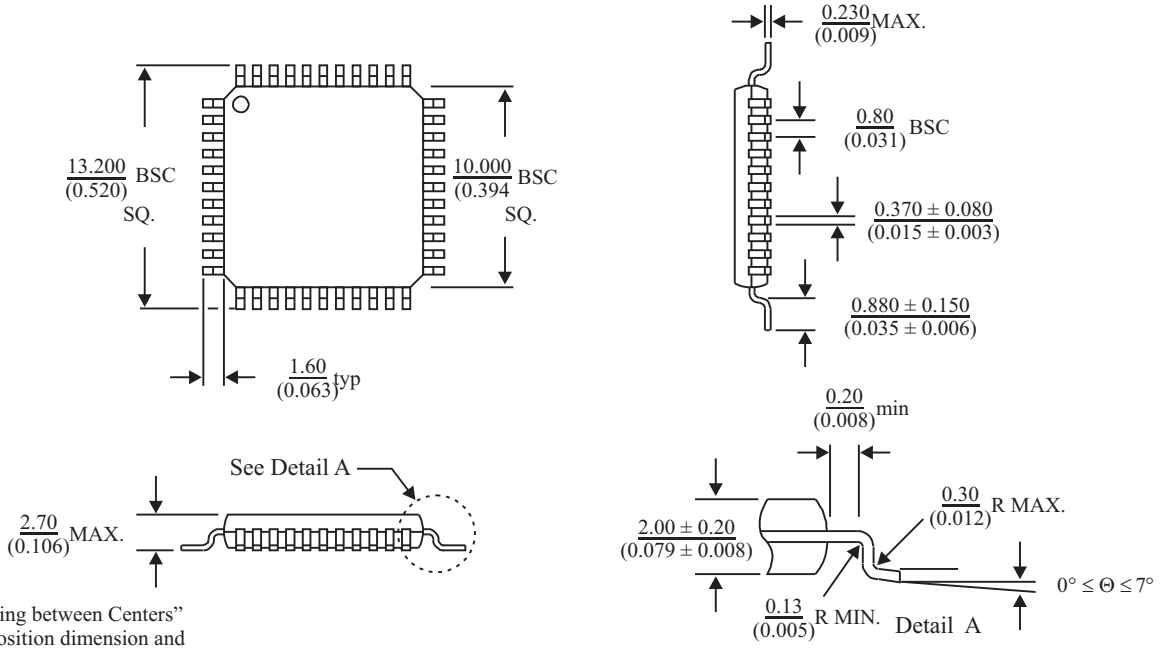


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN PLASTIC QUAD FLAT PACK (PQFP)

millimeters (inches)

Package Type: 44PMQS

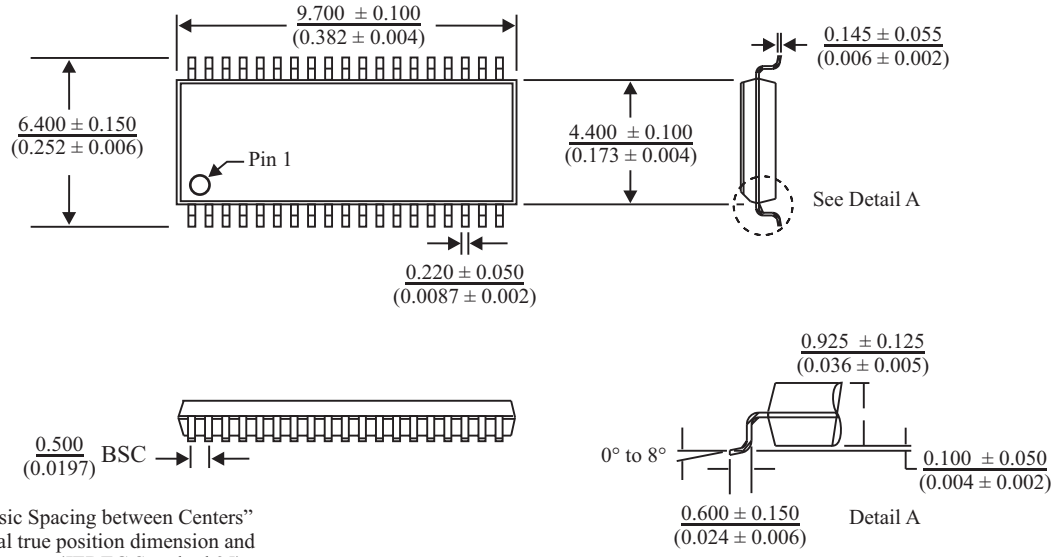


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

38-PIN PLASTIC TSSOP

millimeters (inches)

Package Type: 38HS

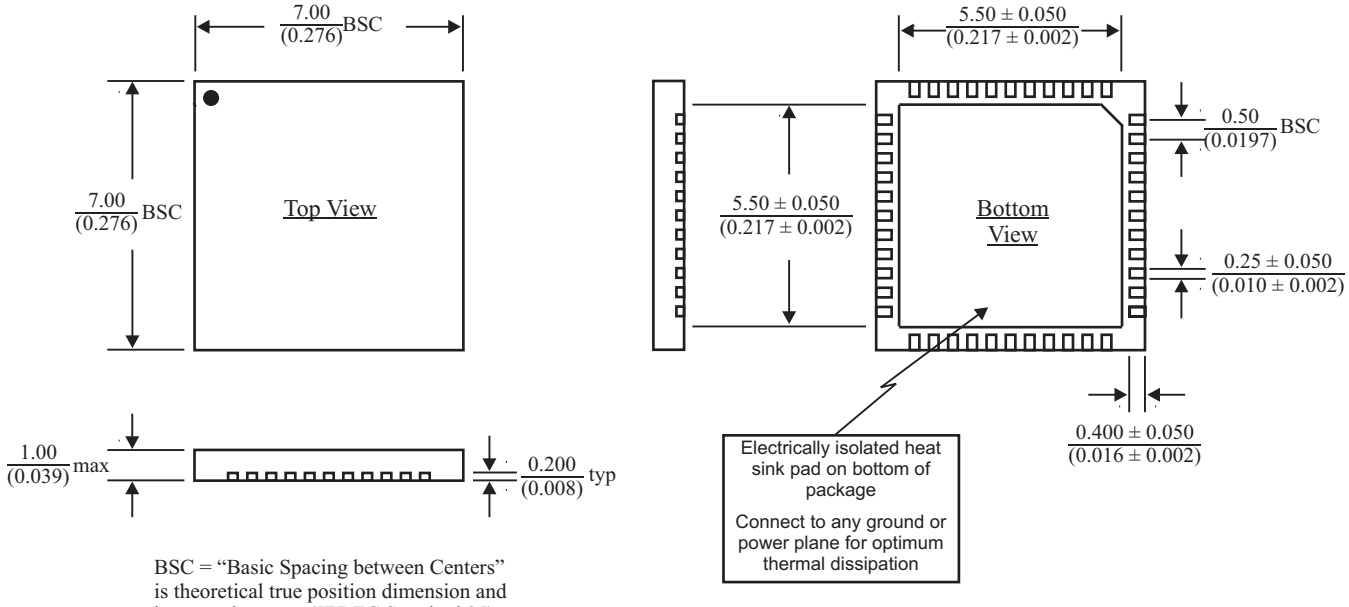


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

millimeters (inches)

Package Type: 44PCS



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