

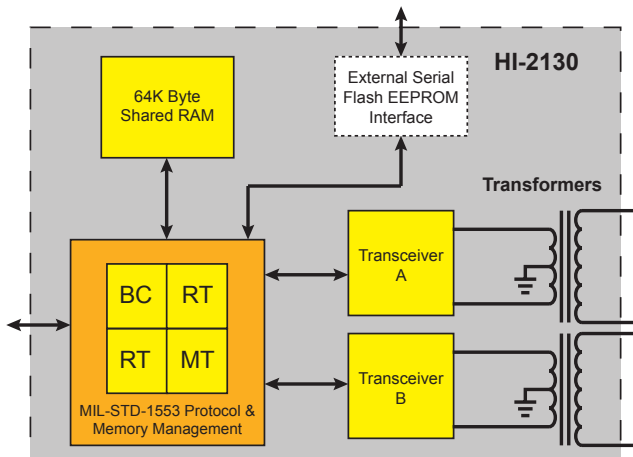
GENERAL DESCRIPTION

The HI-2130 provides a 3.3V fully integrated interface between a host processor and a MIL-STD-1553 / MIL-STD-1760 bus. It combines the functionality of Holt’s HI-6130 16-bit parallel bus interface and HI-6131 SPI devices, integrating MIL-STD-1553 protocol logic, dual transceivers and dual transformers in a single compact 15 x 15mm package. The HI-2130 die is hermetically sealed in a ceramic substrate and dual transformers are mounted onto the same package. Two low profile package options are offered, namely BGA and PGA (see “Ordering Information” on page 7).

The device includes the entire signal I/O set of HI-6130 and HI-6131, with the addition of a new input signal for selecting parallel bus or SPI host interface. Two pairs of transformer output signals connect directly to the MIL-STD-1553 Bus A and Bus B stubs.

The part is available in Industrial -40°C to +85°C, or Extended, -55°C to +125°C temperature ranges. Optional burn-in is available on the extended temperature range.

Refer to the HI-6130 datasheet for full functional description and operation.

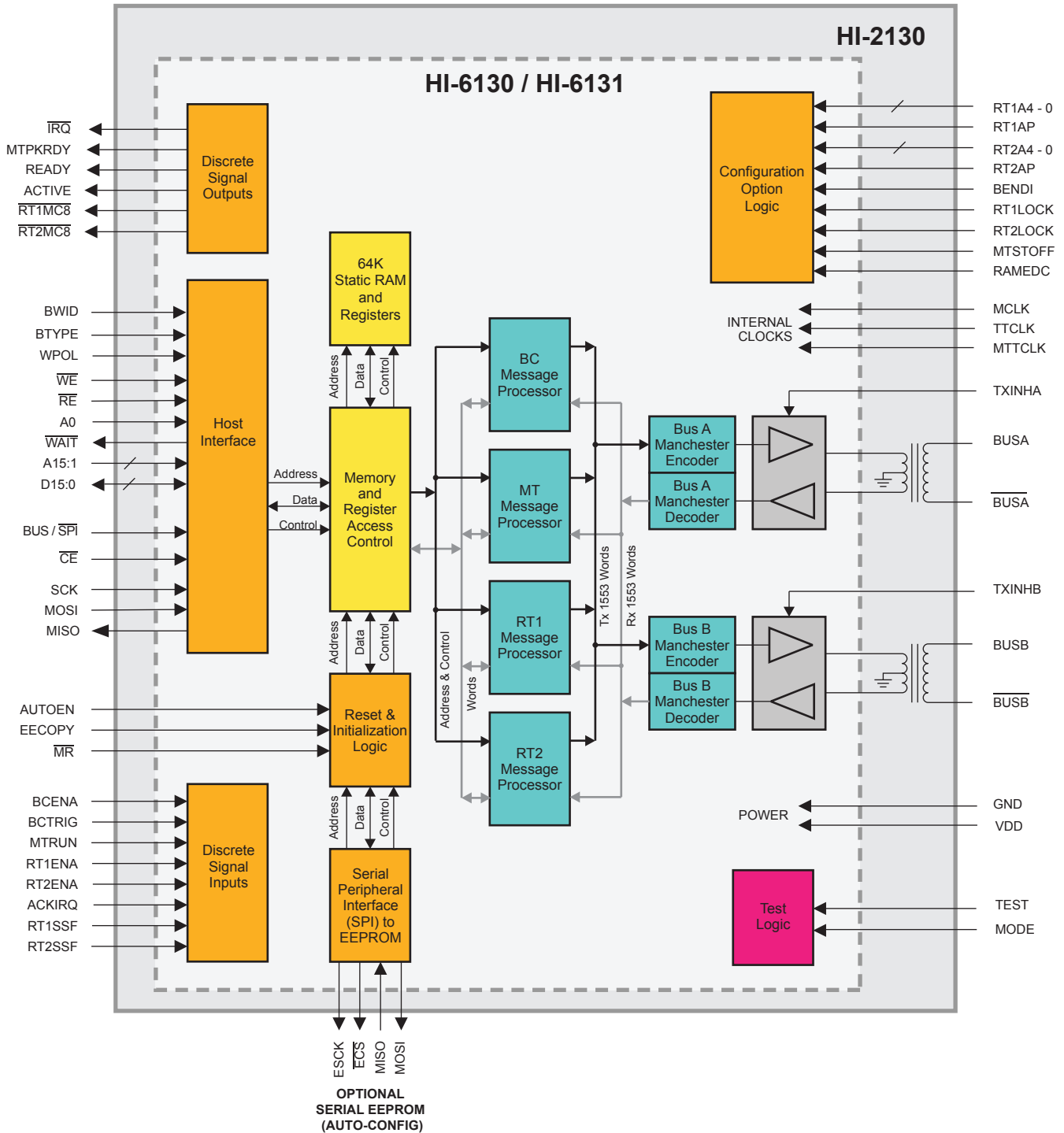


FEATURES

- Combined functionality of HI-6130 and HI-6131 in a single package with integrated transformers
- Smallest footprint MIL-STD-1553 solution available (includes transformers)
- Low profile package solution suitable for PMC and XMC applications
- Extended temperature range, -55°C to +125°C, with optional burn-in
- Hermetically sealed die improves reliability and achieves MSL 1
- Less expensive than traditional multi-chip modules
- DO-254 certifiable
- Concurrent multi-terminal operation (BC, MT, 1 or 2 independent RTs)
- Two host interface options in one package: 16-bit parallel bus or 4-wire SPI
- 64K bytes on-chip RAM with error detection/correction option
- Autonomous terminal operation requires minimal host intervention
- Shared MIL-STD-1553 bus interface reduces circuit complexity and circuit board area.
- Fully programmable Bus Controller with 28 op code instruction set
- Simple Monitor Terminal (SMT) Mode records commands and data separately, with 16-bit or 48-bit time tagging
- IRIG Monitor Terminal (IMT) Mode supports IRIG-106 Chapter 10 packet format. Complete IRIG-106 data packets including full packet headers and trailers can be generated
- Independent time-tag counters for all terminals with 32-bit option for Bus Controller and 48-bit option for Monitor Terminal
- 64-Word Interrupt Log Buffer queues the most recent 32 interrupts. Hardware-assisted interrupt decoding quickly identifies interrupt sources
- Built-in self-test for protocol logic, digital signal paths and internal RAM
- Optional self-initialization at reset uses external serial EEPROM
- Two temperature ranges: -40°C to +85°C, or -55°C to +125°C

HI-2130

BLOCK DIAGRAM



PIN DIAGRAM

Top View

	11	10	9	8	7	6	5	4	3	2	1	
L	RAM EDC	DATA 14	DATA 11	DATA 9	DATA 4	RT1 SSF	MTPKT RDY	RT1 MC8	nIRQ	B TYPE	BENDI	L
K	nCE	DATA 12	DATA 10	AUTO EN	DATA 6	VDD	AC- TIVE	ACK IRQ	DATA 2	WPOL	nBUS A	K
J	MODE	BC TRIG	DATA 13	TX INHA	DATA 7	DATA 5	READY	TEST	DATA 0	DATA 1	nBUS A	J
H	MISO	DATA 15	MOSI	TX INHB	DATA 8	DATA 3	RT2 MC8	MTST OFF	RT1 LOCK	DNC	BUS A	H
G	nWAIT	SCLK	nRE	VDD	GND	VDD	GND	VDD	BC ENA	DNC	BUS A	G
F	nWE	BUS nSPI	MCLK	GND	VDD	GND	VDD	GND	VDD	DNC	DNC	F
E	RT1 A2	RT1 A0	RT1 A1	VDD	GND	VDD	GND	VDD	RT2 ENA	DNC	BUS B	E
D	nMR	RT1 A3	RT1 A4	ADDR 8	nECS	ADDR 10	RT2 LOCK	RT2 A0	RT2 A1	DNC	BUS B	D
C	ADDR 0	RT1 ENA	ADDR 2	E MOSI	GND	EE COPY	MT RUN	RT2 A2	RT2 A3	ADDR 14	nBUS B	C
B	ADDR 1	ADDR 3	ADDR 4	ADDR 6	TT CLK	VDD	ESCK	RT2 SSF	ADDR 13	ADDR 15	nBUS B	B
A	ADDR 5	RT1 AP	E MISO	ADDR 7	MTT CLK	ADDR 9	ADDR 11	RT2 AP	RT2 A4	ADDR 12	BWID	A
	11	10	9	8	7	6	5	4	3	2	1	

See HI-6130 datasheet for a full Pin Description.

Notes:

- a. DNC: Do Not Connect.
- b. All balls denoted VDD **must** be connected to 3.3V DC power.
- c. All balls denoted GND **must** be connected to circuit ground.
- d. BUS/nSPI (F10) selects 16-bit wide parallel bus or SPI operation (see Section “Selection of Host Interface” on page 4).
- e. nCE: The chip enable signal is shared between 16-bit parallel and SPI host interfaces (SPI Slave Select).

OPERATION

Refer to the HI-6130 datasheet for detailed operation and register description.

Selection of Host Interface

The host interface is selected using the SPI/ $\overline{\text{BUS}}$ pin.

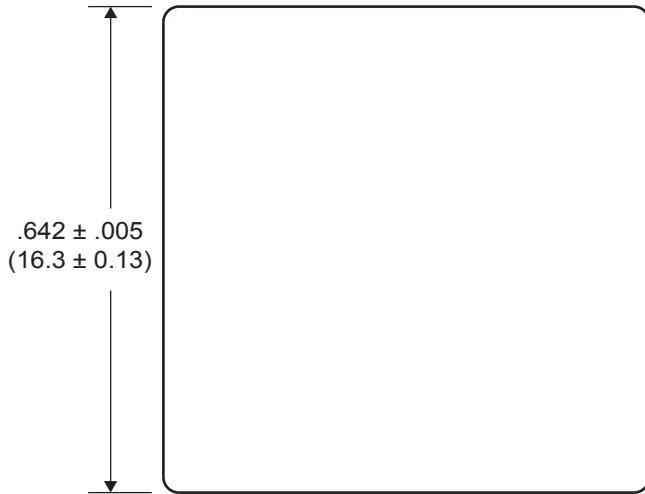
- BUS/ $\overline{\text{SPI}}$ pin set to logic "1": Selects 16-bit parallel bus host interface
- BUS/ $\overline{\text{SPI}}$ pin reset to logic "0": Selects SPI host interface

PACKAGE DIMENSIONS

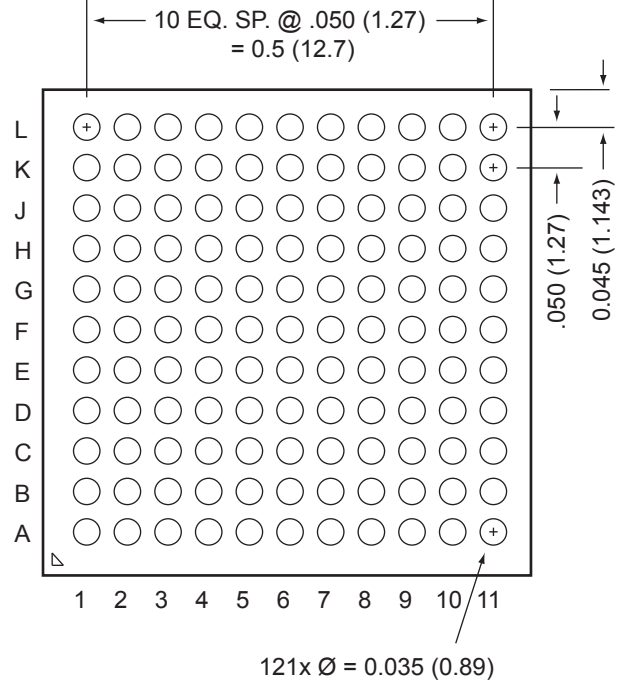
Ball Grid Array

inches (millimeters)
Package Type: 121BGA2

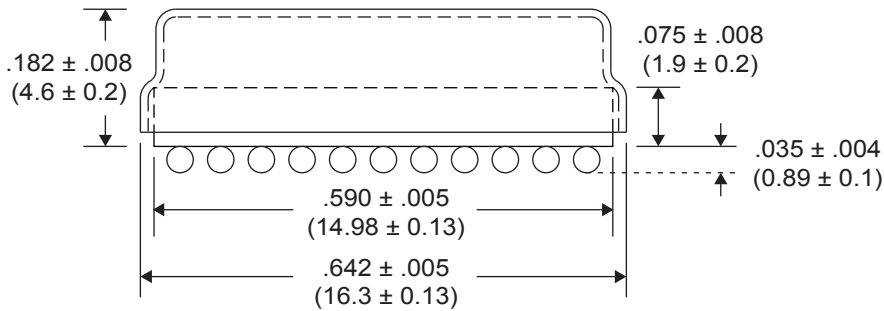
Top View



Bottom View



Side View

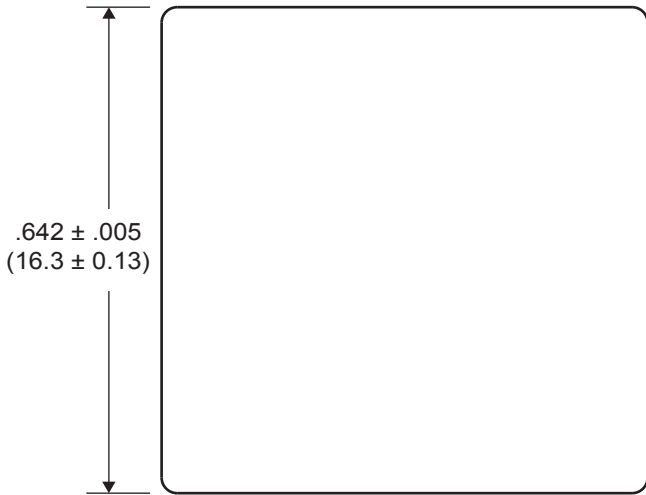


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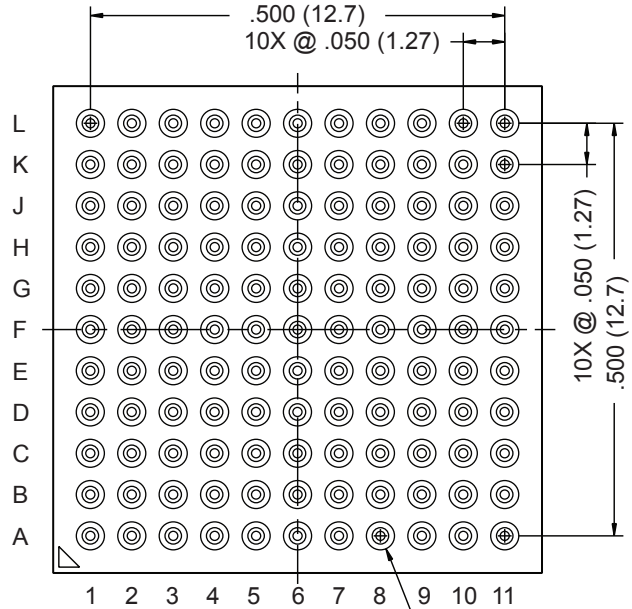
Pin Grid Array

inches (millimeters)
Package Type: 121PGA2

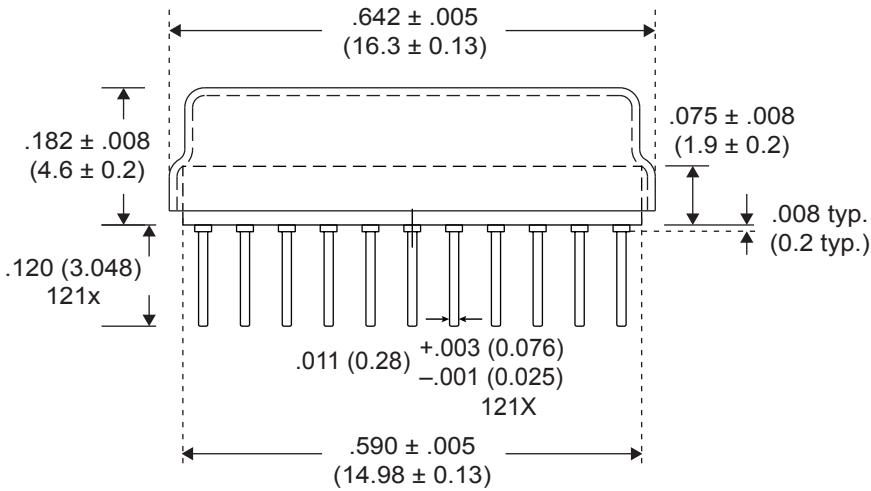
Top View



Bottom View



Side View



121X $\varnothing.0338$ $^{+0.0020}$
 $_{-0.0019}$

$\varnothing.012$ (M)	C	A	B
$\varnothing.006$ (M)	C		

inches

HI-2130

ORDERING INFORMATION

HI - 2130 Gx x F

PART NUMBER	LEAD FINISH
F	Pb-free, RoHS compliant

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No

PART NUMBER	PACKAGE DESCRIPTION
GP	121 PIN GRID ARRAY - PGA (121PGA2), (Pb-free, RoHS compliant)
GB	121 BALL GRID ARRAY - BGA (121BGA2), non-collapsing solder balls

HI-2130

REVISION HISTORY

Revision	Date	Description of Change
DS2130, Rev. New	09/14/12	Initial Release.
Rev. A	11/14/12	Corrected typos in pin diagram. Updated package drawings for new thickness. Updated Ordering Information table.
Rev. B	01/22/13	Remove LGA package option.
Rev. C	07/28/14	Remove leaded BGA option.
Rev. D	03/18/15	Replace "CB" and "CP" package options with low profile "GB" and "GP" package options.
Rev. E	05/28/15	Remove dimensions from front page package drawing.